## SPACEWIRE REMOTE TERMINAL CONTROLLER

**Session: SpaceWire Components** 

## **Short Paper**

Jørgen Ilstad, Wahida Gasti

European Space Agency, Postbus 299, NL-2200 AG Noordwijk, The Netherlands

Peter Sinander

Saab Space AB, SE-40515 Göteborg, Sweden

Sandi Habinc

Gaisler Research AB, Första Långgatan 19, SE-41327 Göteborg, Sweden

E-mail: jorgen.ilstad@esa.int, wahida.gasti@esa.int, peter.sinander@space.se, sandi@gaisler.com

## **ABSTRACT**

The SpW Remote Terminal Controller (RTC) ASIC is a single chip embedded system that includes a general purpose LEON2-FT SPARC V8 core with a MEIKO FP unit (IEEE-754). This architecture provides the mixed capability to effectively perform data handling at platform level and powerful data processing capability at payload level. Depending on its application in a design it supports remote control and configuration of the device. Indeed it is based judiciously on:

- LEON2-FT SPARC V8 with MEIKO FP unit.
- Appropriate amount of on-chip memory EDAC protected 64k SRAM, and EDAC protected interfaces to external memory devices such as SRAM, (EE)PROM and FIFO.
- Two SpaceWire interfaces (compliant to SpW IP codec ECSS-E-50-12A and RMAP IP / ECSS-50-11) a Controller Area Network (CAN IP HurriCANe) bus controller
- ADC/DAC (16bit) for payload data acquisition/conversion.
- Standard interfaces and resources (UARTs, 32bit timers, JTAG, general purpose input and output). It can provide up to 96 I/O lines as general purpose signals depending on its application.

The RTC complies with very challenging scientific requirements established by science teams in order to minimize payload front-end power consumption while increasing its performances. Accordingly, it is considered as a potential candidate for ESA programs such as Bepi-Colombo, XEUS, Cosmic Microwave Background Polarization Mapper (CMPM), to name a few.

After a brief description of the chip and its capabilities, this paper presents a set of architectures where the RTC is well suited. Focus will be on the low power-high performances capability of the derived architectures, taking into account scientific requirements for deep space science missions.