"MCFLIGHT" – THE CHIPSET FOR DISTRIBUTED SIGNAL PROCESSING AND CONTROL WITH SPACEWIRE INTERCONNECTIONS

Session: SpaceWire Components

Long Paper

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ABSTRACT

The article presents the "MCFLIGHT" family of chips for distributed architectures with SpaceWire interconnections for signal processing and control. The chipset chips was developed for aerospace on-board data processing and control systems on the base of customizable System-on-Chip (SOC) design and is produced by the "ELVEES" RnD Center (Moscow). Main features and characteristics of the chips are presented.

1. INTRODUCTION

The chipset "MCFLIGHT" was developed for aerospace on-board data processing and control systems on the base of modern technology of customizable System-on-Chip (SOC) design. It includes 5chips, Table 1, for building distributed architectures with SpaceWire interconnections.

Table 1. Chipset "MCFLIGHT" with SpaceWire for aerospace applications

Chip		Type
	**MC24R**	**Dual-core DSP**; 600MFLOPs peak performace; 2 embedded **SpaceWire** links, 5-400 Mb/s
	**MCT01**	**Peripheral controller** RISC-core (MIPS32-64FP); 4-channel ADC/DAC; 2 embedded **SpaceWire** links, 5-400 Mb/s
	**MCB01**	**Bridge** **SpaceWire** /PCI/Memory bus, 4 SpaceWire links, 5-400 Mb/s embedded SRAM 2 Mb
	**MCK01**	16-channel **SpaceWire routing switch**; SpaceWire links 5-400 Mb/s, embedded RISC-core (MIPS32 architecture); Processor bus; Memory bus.

The chipset incorporates ideas of multi-core chips with RISC- and DSP-cores, new high-rate on-board communication technology SpaceWire, scalable distributed

architecture support and advanced embedded software for real-time parallel processing and control in distributed architectures. The chipset includes the high-performance multicore (RISC + DSP cores) processors MC24R with embedded SpaceWire links, the control processor MCT01 with embedded SpaceWire links, the 16-port SpaceWire routing switch MCK01, the 4-channel SpaceWire bridge for PCI bus and Memory access bus. Chips are produced in 0,25 un technology. Used in these chips IP-blocks of SpaceWire link controllers (NICs) run with rates up to 400 Mbit/s and implement extended version of the SpaceWire standard with Interrupt/IntAknowledge codes support. SpaceWire NICs are supported by drivers in Linux that run on the chips. Integrated software development package MCStudio is provided for software development and debugging.

2. DUAL-CORE DIGITAL SIGNAL PROCESSOR MC24R

Digital signal processor MC24R was designed for application in on-board control and data systems. It is the heterogeneous dual-core processor chip: a 32-bit DSP-core for high-performance signal and data processing and a 32-bit RISC-core for control and scalar data processing. Its structure is presented at the fig. 1., its main characteristics in the Table. 2.

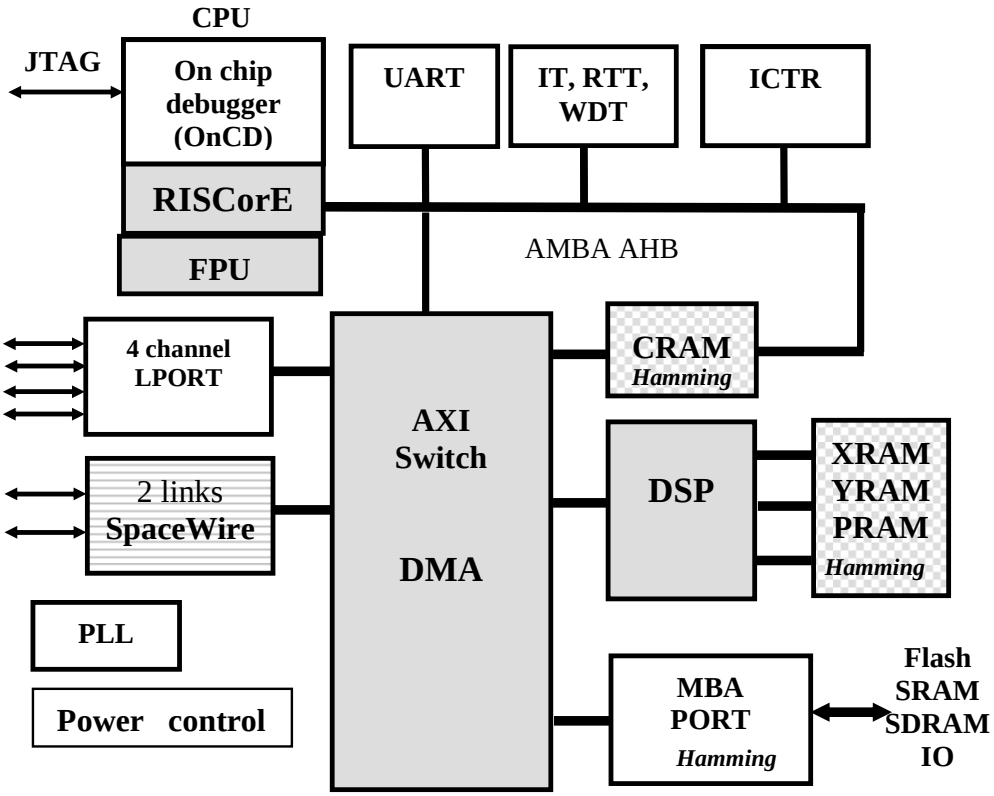

Fig. 1. Digital signal processor MC24R structure

The DSP-core has the original microarchitecture ELcore-24, which is optimized for massive signal and vector data processing, incorporates VLIW, pipelining, macro load/store and 2-way SIMD architecture features. It also includes 3 high-rate memory blocks with parallel access for DSP-core program codes (PRAM) and data (XRAM and YRAM). The 32-bit RISC-core has MIPS32-compatible architecture, with a cash and FPU, but is the originally designed by ELVEES processor core. Low latency

memory CRAM stores RISC-core program codes and data. The 16-channel DMA-core supports multiple data flows inside the chip and with off-chip components.
One of the MC24R specifics is extended support for building distributed on-board systems. Embedded in the MC24R 2 SpaceWire links provide duplex information flows with rates up to 400 Mb/s each. They ensure interfacing the MC24R with remote sensors and information flow recipients. It can be directly connected to other SpaceWire-compliant devices, routing switches included (e.g. MCK-01). Thus the MC24R is a ready-made component for building distributed on-board systems with SpaceWire based interconnections.

The chip was design with the "Rad Hard By Design" methods, with 0,25 μn CMOS technology. For fault-tolerance Hamming coding is used also.

Table 2. Digital signal processor MC24R characteristics

Technology	CMOS ASIC, 0,25 μn/ 5metal layers, 3,3 V (peripherals) / 2,5 V (core)
Frequency	100 MHz for the RISC-core 200 MHz for the DSP-core
RISC– core	32-bit, MIPS32-compatible architecture Performance 100 Mips Instructions cash – 16 Kbytes
FPU	Works in parallel with the main RISC-core, single and double ANSI/IEEE754 flow point operations.
DSP-core	Original microarchitecture ELcore-24. Peak performance: 600 Mflop– 32-bit IEEE754, 3600 Mips – 8-bit fixed point, 1600 Mips - 16-bit fixed point 800 Mips – 32-bit fixed point
On-chip memory	CRAM: 32 Kbytes (dual-prt) XRAM, YRAM 64 Kbytes PRAM 16 Kbytes
Memory port (MBA)	Address bus - 32 bits, Data bus - 64 bits Supports SRAM, Flash, SDRAM (100МГц) Programmable wait cycles; 4 interrupt lines. 4 external DMA requests
SpaceWire links	2 SpaceWire links Compliant with the ECSS-E-50-12A standard, with extensions (distributed interrupts). 5-400 Mb/s. LVDS-signals (ANSI/TIA/EIA-644).
Other interfaces	4 byte-wide ports (compliant with ADSP21160), . GPIO mode. UART: UART 16550 type, 50 baud – 1Mbaud. JTAG IEEE 1149.1
OnCD	On-chip debug facilities, access through JTAG IEEE 1149.1.
Power saving modes	Several modes for power saving, programmable.
Fault tolerance	All memory blocks are protected by modified Hamming code
Package	HSBGA-416

3. PERIPHERAL CONTROLLER MCT01

Peripheral controller MCT01 was designed as a terminal controller of distributed on-board systems for direct interfacing with on-spacecraft equipment and payload instruments. For interfacing the MCT01 has 4 channels of ADC and 4 channels of DAC, GPIO pins, UART. The MCT01 structure is presented at the fig. 2. and its main characteristics in the Table. 3.

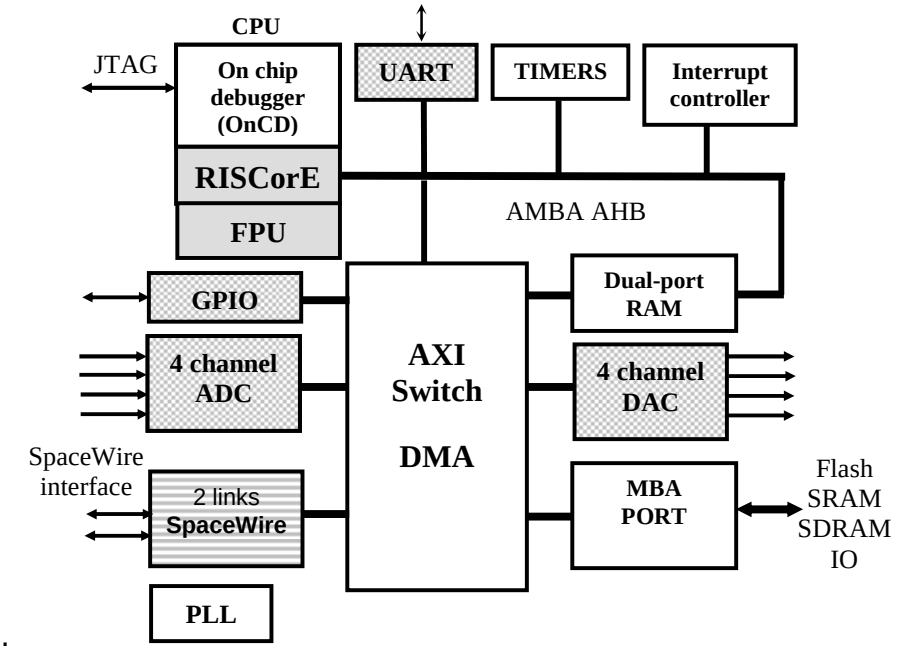

Fig. 2. Peripheral controller MCT01 structure

For local control, medium rate signal and data processing the MCT01 has the MIPS32-compatible 32-bit RISC-core, with a cash and FPU. There is on- dual-port SRAM for program codes and data. The RISC-core with FPU are similar to the RISC-core in the MC24R. Additional memory and IO devices can be attached by the programmable MBA port. Two 2 SpaceWire links embedded in the MCT01 provide duplex information flows with rates up to 400 Mb/s each. Thus MCT01 can be directly connected to other SpaceWire-compliant devices, routing switches included, processors, other peripheral controllers, as well as to instruments and sensors with embedded SpaceWire links. As the other **"**MCFLIGHT**"** chips MCT01 is a ready-made component for distributed on-board systems with SpaceWire interconnections.

Table 3 Peripheral controller MCT01 characteristics

Technology	CMOS ASIC, 0,25 μn/ 5metal layers, 3,3 V (peripherals) / 2,5 V (core)
Frequency	100 MHz
RISC– core	32-bit, MIPS32-compatible architecture Performance 100 Mips Instruction/Data cash – 16 Kbytes/16 Kbytes
FPU	Works in parallel with the main RISC-core, single and double ANSI/IEEE754 flow point operations.

On-chip memory	SRAM: 62 Kbytes (dual-port)
DMA	16 channels
32-bit timers	Interval timer; Real-time timer;Watchdog timer
Memory port (MBA)	32 bits, Supports SRAM, Flash, SDRAM (100 MHz) Programmable wait cycles; 4 interrupt lines. 4 external DMA requests
SpaceWire links	2 SpaceWire links Compliant with the ECSS-E-50-12A standard, with extensions (distributed interrupts). 5-400 Mb/s. LVDS-signals (ANSI/TIA/EIA-644).
Other interfaces	GPIO 16 bits. UART: UART 16550 type, 50 baud – 1Mbaud. JTAG IEEE 1149.1
OnCD	On-chip debug facilities, access through JTAG IEEE 1149.1.
ADC/DAC	4 channels, 13 bits, 1 Mhz.
Package	BGA-292

4. MULTI-CHANNEL BRIDGE MCB01

The MCB01 (MultiCore Bridge) is a multipurpose chip for interfacing processors and subsystems, which have not a SpaceWire interface, with SpaceWire interconnections. It can be also used to extend number of SpaceWire links, e.g. extend number of SpaceWire links of a MC24 based unit from2 to 6. The MCB01 structure is presented at the fig. 3. and its main characteristics in the Table. 4.

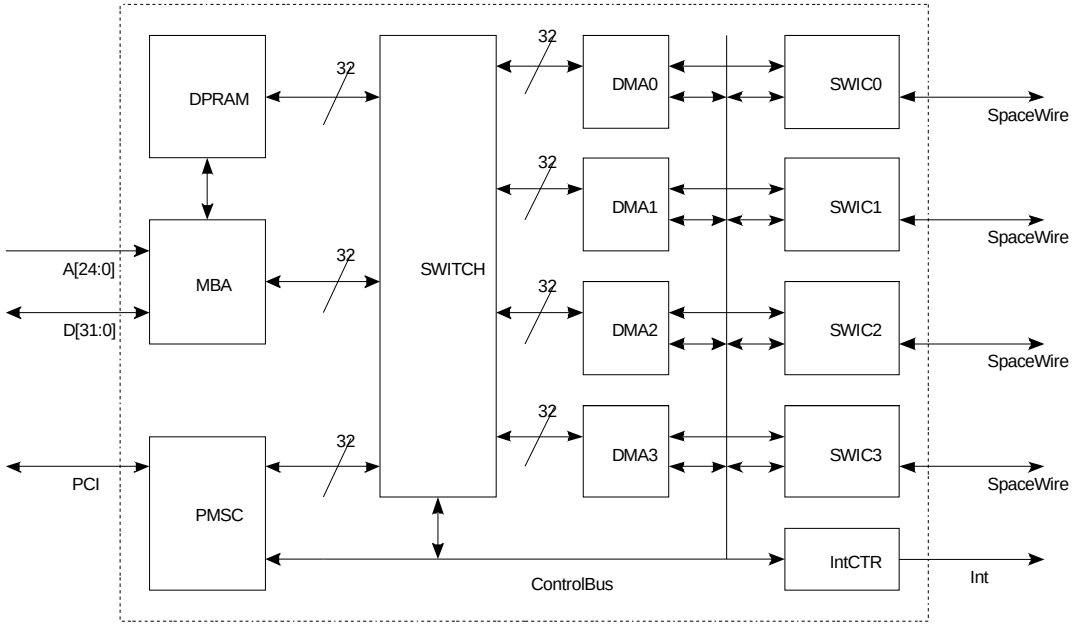

Fig. 3. Multi-channel bridge MCB01 structure

MCB01 has 4 independent SpaceWire link controllers, SWIC0 – SWIC3. They work in parallel and have independent operation mode control, link transmission rates included. SpaceWire links controllers generate signals on a set of events in the links operation (connection/disconnection; parity error; EOP, time-code, interrupt-code

receipt; etc.). They are stored in the links' status registers and can be transferred to a host by interrupt signals (can be masked), both to MBA and PCI ports.
From the side of a host the MCB01 provides two types of parallel interfaces: the MBA port (a typical for microcontrollers bus) and the PCI bus interface. By the MBA port the MCB01 can be attached, for instance, to all the processor and controller chips of the "MCFlight" family. By the standard for industry PCI port it can be connected with a vast variety of chips, computers and systems that use PCI bus. The PCI port (slave) can operate in 32 bit or 64 bit modes, at 33 or 66 MHz. The MCB01 architecture supports simultaneous hosts operation by the MBA and the PCI ports.
Embedded MCB01 dual port high-rate memory (128 Kbytes) supports full rate operation of all the 4 duplex links. The SpaceWire link controllers work with the memory by embedded in them multi-channel DMA. From the host side, the MCB01 embedded memory and registers of the SWICs are represented in the host memory address space (both from the MBA and from the PCI sides).

Table 4. Multi-channel bridge MCB01 characteristics

Technology	CMOS ASIC, 0,25 μn/ 5metal layers, 3,3 V (peripherals) / 2,5 V (core)
SpaceWire	**4** SpaceWire links. Independent link operation modes and transmission rates programming Compliant with the ECSS-E-50-12A standard, with extensions (distributed interrupts). 5-400 Mb/s. LVDS-signals (ANSI/TIA/EIA-644).
Memory port (MBA)	32 bits data bus, 25 bits address bus, 100 MHz)
PCI	PCI bus port (slave); Local Bus Specification. Rev. 2.2. 32-bit and 64 bit modes; 33 MHz / 66 MHz;
On-chip memory	SRAM 128 Kbytes (64Kx32), dual-port, up to 100 MHz
Package	HSBGA-416

5. SPACEWIRE ROUTING SWITCH MCK01

The MCK01 chip is the 16-channel SpaceWire routing switch. It was designed as the "MCFLIGHT" basic component for building scalable SpaceWire interconnections for on-board aerospace systems. The MCK01 is designed in conformance with the SpaceWire layered protocol stack. It can be used for interconnections between processing modules of parallel and distributed data and signal processing systems, as well as for organizing programmable interconnection between sensors/actuators and processing/control on-board computers. It provides efficient, low latency switching for different types of information flow: from heterogeneous flows of short packets (typical for inter-module traffic in parallel processing and distributed control) up to continuous homogeneous data flow from sensors to DSP. The MCK01 structure is presented at the fig. 4. and its main characteristics in the Table. 5.
MCK01 has 16 SpaceWire links with individually programmable mode of operations and transfer rates. 16 parallel link controllers and non-blocking switch provide high throughput and low latency packets and control codes switching through the router.
The MCK01 implements in hardware wormhole routing with all the specified by the SpaceWire standard addressing modes: path, logical, regional-logical addressing. It is

supported by the programmable full scale routing table in the chip. The MCK01 supports adaptive routing also, thus providing a mechanism for information flow distribution between multiple terminal nodes, with automatic dynamic information flows redistribution between channels, adaptation to channel faults for reliable on-board system configurations with redundancy.

For building real-time distributed systems the MCK01 supports an extended set of control codes. Along with the specified by the ECSS-E-50-12A standard time-codes it implements also the distributed Interrupt/Interrupt Ack codes that were proposed for the next release of the SpaceWire standard. As much as 32 Interrupt codes can be simultaneously distributed with low latency and without blocking or retarding by data flows in a SpaceWire interconnection with the MCK01 switches.

This routing switch is an intelligent one. While multi-megabit packet flows on 16 duplex links are processed by the MCK01 in hardware, on the fly, it has the embedded RISC-processor core also.

The configuration port (port 0) is assigned to the RISC-core unit. Thus the MCK01 has particular facilities for scalable intelligence and adaptability for application environments as well as to evolution of SpaceWire family standards. For instance, a PnP protocol that is under development now by the SpaceWire community, whatever final form it will have, will be readily implemented in firmware of the MCK01 that is in production already; it could be doped even into an installed and operating equipment or instrument with MCK01 inside.

Two parallel ports expand the MCK01 intelligence scalability and flexibility of its application in systems with different requirements and configuration. By the MPORT (master) additional memory (SRAM, Flash, SDRAM) or peripherals can be attached to be accessed and controlled by the embedded RISC-core. By the MBA (slave) external processor can interface the MCK01 for data interchange and taking control over the MCK01 operation. It will have access to the embedded memory and registers of the MCK01 that will be seen in its memory address space. The UART port makes interfacing the MCK01 to external test, debug or monitoring tools quite easy.

Table 5. SpaceWire routing switch MCK01characteristics

Technology	CMOS ASIC, 0,25 μn/ 5metal layers, 3,3 V (peripherals) / 2,5 V (core)
SpaceWire links	16 SpaceWire links Compliant with the ECSS-E-50-12A standard, with extensions (distributed interrupts). 5-400 Mb/s. LVDS-signals (ANSI/TIA/EIA-644).
RISC– core	32-bit, MIPS32-compatible architecture Performance 100 Mips
Frequency	100 MHz for the RISC-core Individually programmable frequencies of the 16 SpaceWire links
On-chip memory	SysRAM: 16 Kbytes Routing table 1 Kbyte Packet RAM(for cofiguration port) 8 Kbytes
MBA	Slave. 32 bits.
MPORT	Master. 32 bits; Supports SRAM, Flash, SDRAM (100МГц) Programmable wait cycles;
Other interfaces	UART: UART 16550 type, 50 baud – 1Mbaud. JTAG IEEE 1149.1
OnCD	On-chip debug facilities, access through JTAG IEEE 1149.1.
Package	HSBGA-416

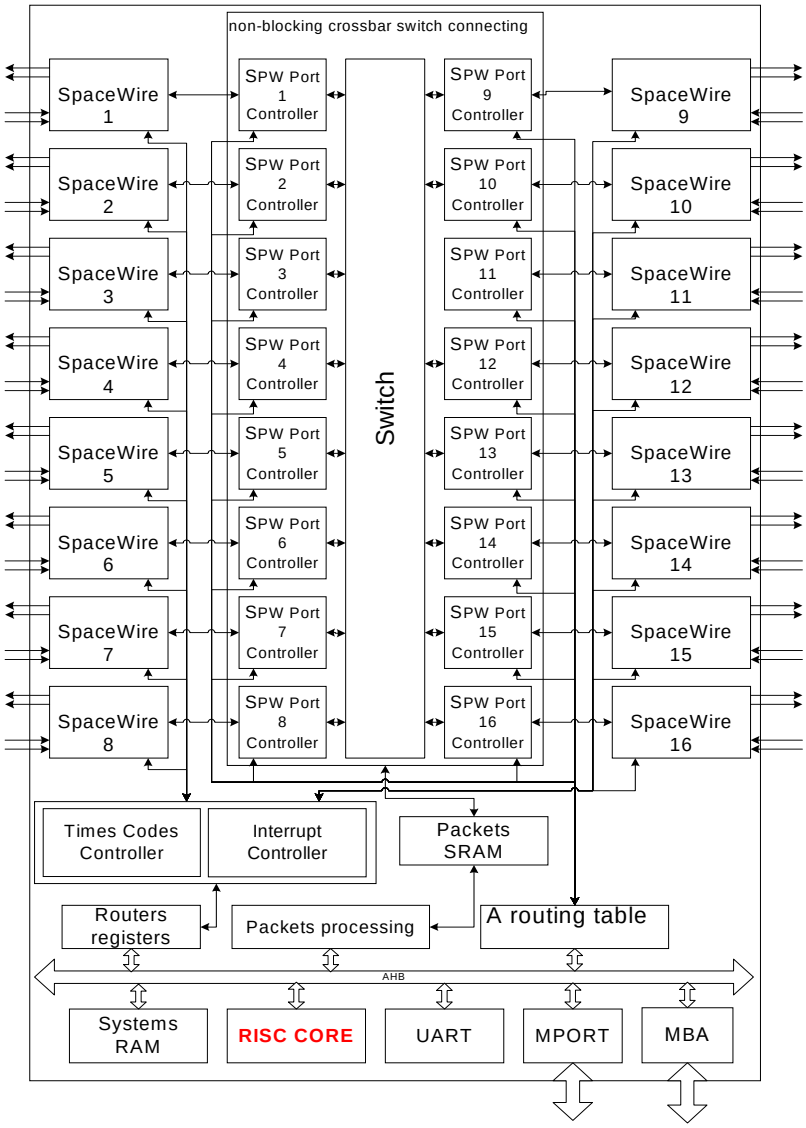

Fig. 4. SpaceWire routing switch MCK01structure

Conclusions

1. The engineering samples of MCFlight - “MULTICORE” platform based chipset (0.25-u) with SpaceWire links for distributed aerospace systems have been received and its functionality is proved on the HW modules;
2. ASICs and FPGA SpaceWire Links provide up to 400 Mbps and higher throughput (>5m) in the cross modules connections;
3. Chipset provides a lot of the innovational features and supports high performance, programmability, scalability and flexibility;
4. A lot of ELVEES ‘s technologies for “MULTICORE” platform (SDR, Adaptive signal/image processing , 3D graphics , Networks information security, multimedia, Intellectual systems of video observation) will be transferred on the MCFlight chipset;
5. MCFlight can be easily modified (during some months) by others platforms IP-cores (for example, for SPARC RISC core) or for others interfaces.