SpaceWire-RTC Development Suite

Session: Onboard equipment and software

Short Paper

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ABSTRACT

The objective of the SpaceWire Remote Terminal Controller (SpaceWire-RTC) ASIC development has been to provide the European space industry with a single-chip solution for their SpaceWire and Controller Area Network (CAN) needs for the decade to come. With the ASIC development nearing its completion, the next challenge is to provide the users with a complete development suite to simplify the hardware and software design of applications using the SpaceWire-RTC ASIC.

1 SPACEWIRE REMOTE TERMINAL CONTROLLER ASIC

The SpaceWire-RTC ASIC [1] comprises the following functions:

- LEON2-FT 32-bit Fault Tolerant SPARC Processor and MEIKO FPU
- Debug Support Unit with Debug Serial Link UART
- Primary and Secondary Interrupt Controllers
- 32-bit Timers
- UART Serial Links
- 16-bit General Purpose Input Output
- 32-bit Memory Interface with EDAC support
- 64 kByte EDAC protected On-Chip Memory
- 8/16-bit FIFO Interface
- 16-bit ADC/DAC Interface
- 32-bit Timers, with external clock source and triggers
- 24-bit General Purpose Input Output with pulse generation
- CAN 2.0 Interface, with redundant interfaces
- 2x SpaceWire Link Interfaces

The ASIC has been designed using Intellectual Property (IP) [2] cores from various sources [6] [7]. The on-chip architecture is based on the AMBA AHB and APB on-chip buses that have been extended with a plug&play capability [3]. The ASIC will be manufactured by Atmel in their 0.18 um ATC18RT process and will be packaged in a MCGA 394 package. The ASIC has been designed by Gaisler Research and the prime Saab Space AB.

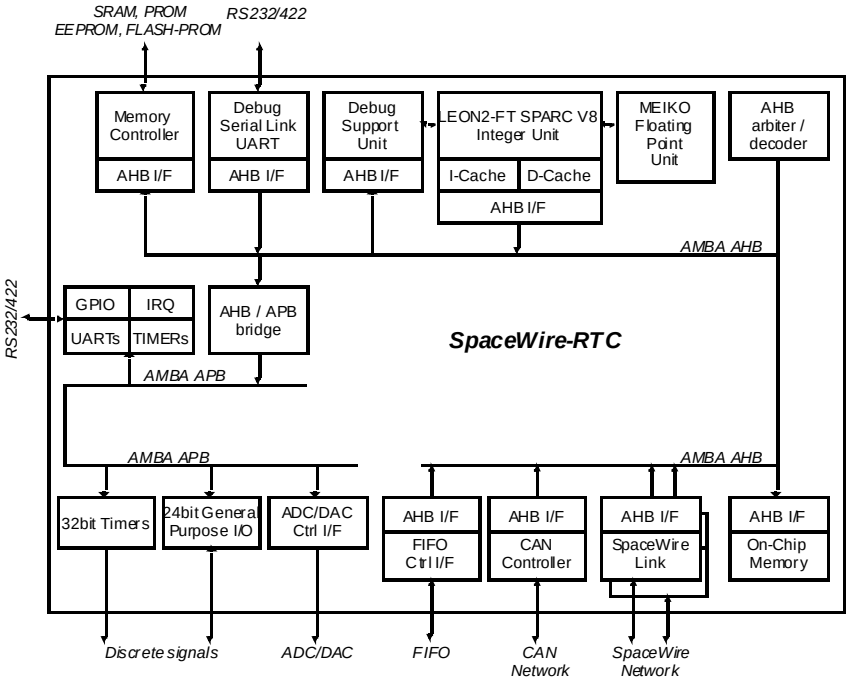

Figure 1. SpaceWire-RTC block diagram

2 SPACEWIRE-RTC DEVELOPMENT SUITE

The SpaceWire-RTC Development Suite is composed of several elements covering hardware, software and development tools. The objective is to provide the customers with a ready-to-use off-the-shelf product.

The development suite comprises the following elements:

- Hardware:
  - ASIC development board with housing
- Software:
  - LEON Bare-C Cross Compilation System (BCC)
  - RTEMS Cross Compilation System (RCC) - BSP and drivers
  - VxWorks – BSP and drivers
- Tools:
  - GRMON - debug monitor
  - GRESB - Ethernet to SpaceWire and CAN bridge
  - TSIM2 - instruction simulator with a loadable SpaceWire-RTC module

Each element is described in detail in the subsequent sections.

3 HARDWARE

The ASIC development board comprises all the memory, interfaces, transceivers and connectors that a designer would need. The board is enclosed in a housing to simplify its handling, but a can also be used without the housing and allows for expansion.

The development board comprises:

- SpaceWire-RTC ASIC
- On board Memory: SRAM / FLASH / EEPROM / PROM socket
- Interface driver circuits and connectors for UART, CAN and SPW interfaces
- 12 bit DAC (1 channel) and 12 bit ADC (4 channel input Multiplexer)
- FIFO circuits for 8/16 bit FIFO high-speed data transfer
- General Purpose Timer triggers
- On-Board Oscillators plus connectors for injecting external clocks
- DIP Switches, Push Button switches and LED indicators for configuration
- Power Supply Circuits

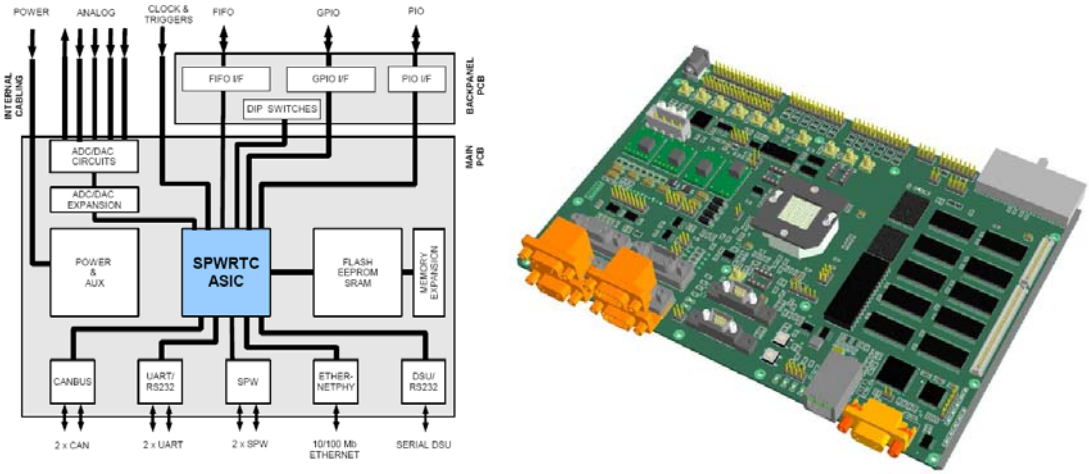

Figure 2: SpaceWire-RTC Development Suite Hardware

4 SOFTWARE

The two operating systems explicitly supported by the SpaceWire-RTC development suite are RTEMS and VxWorks. Although the two operating systems are provided under very different conditions, one being commercial and the other being for free, they have much in common concerning board support packages and drivers.

The RTEMS Cross Compilation System (RCC) [11] already includes support for the LEON2 and LEON2-FT processors. The following SpaceWire-RTC ASIC features are therefore already covered by RCC:

- LEON2-FT Integer Unit with MEIKO Floating Point Unit
- LEON2 Memory Interface
- LEON2 Debug Serial Link UART
- LEON2 UART Serial Links
- LEON2 34-bit Timer
- LEON2 16-bit General Purpose Input Output
- LEON2 Interrupt Controller

Newly developed drivers cover the following features of the ASIC:

- FIFO Interface
- CAN Interface
- SpaceWire Link Interface

The following SpaceWire-RTC ASIC features are covered by newly developed structures and functions:

- LEON2 Secondary Interrupt Controller
- On-chip Memory
- 32-bit Timers
- 24-bit General Purpose Input Output
- ADC/DAC Interface

The existing LEON2 Board Support Package (BSP) is re-used for the SpaceWire-RTC ASIC. It only required minor configuration changes to support this device. RTEMS version 4.6.5 is supported.

Similarly, VxWorks already includes supports for the LEON2 and LEON2-FT and therefore required a similar set of drivers, structures and functions to be developed for the SpaceWire-RTC ASIC. VxWorks version 5.4 is supported [12].

5 TOOLS

The tools explicitly supported by the SpaceWire-RTC development suite are GRMON, GRESB and TSIM2.

GRMON [9] is a debug tool that can communicate with the SpaceWire-RTC ASIC either via the Debug Support Link or via the RMAP protocol over the SpaceWire links. Since GRMON has been used during the development of the ASIC, the tool has been constantly adapted to support the ASIC fully. It requires therefore no updating.

The same applies to the GRESB Ethernet to SpaceWire bridge [10]. The GRESB allows communication with SpaceWire links through Ethernet, supporting functions such as SpaceWire packet routing, IP tunneling, remote debugging of LEON3 and LEON2 processors, etc. It required no update to support the SpaceWire-RTC ASIC.

TSIM2 is a simulator that can emulate LEON2 based computer systems [8]. It can also emulate user specific system-on-a-chip solutions by means of loadable modules. TSIM2 allows emulation of the LEON2 processor core with a completely user-defined memory and I/O architecture. The emulated processor core communicates with the AHB module using an interface similar to the AHB master interface in the real LEON2 VHDL model. The AHB module can then emulate the complete AHB bus and all attached units.

A TSIM2 loadable module has been developed to allow simulation of the SpaceWire-RTC ASIC. Note that only newly added functions needed to be developed in the loadable module, since TSIM2 already models the core of the LEON2 system including its peripherals.

6 CONCLUSIONS

The innovative contents of the work presented is to establish a development environment that combines software tools, hardware and test equipment in one package, with possibility for extension with user hardware or software, but still simple enough for office use (software development). This approach has been used in commercial activities and products of Gaisler Research and has now been employed in the space sector as well.

The resulting product has direct usefulness for space applications such as ESA's Bepi-Colombo programme where SpaceWire-RTC based instruments are being considered. The result will have a direct application to the development of software and hardware in projects where the SpaceWire-RTC ASIC will be used, fulfilling ESA's needs for a powerful hardware and software development suite.

The substantial improvement over existing technologies can be seen in the product integration aspect, where ease of use and turnkey solutions has been the leading goal. The benefits of programmatic improvements in terms of one complete development suite provided by a single support house should not be overlooked. It is rare that an SME has the in-depth knowledge about both hardware and software for a space component. The SpaceWire-RTC development suite puts the customer in focus. Instead of developing a board that only fits one system house, the development suite addresses multiple customers with varying needs.

7 REFERENCES

1. Jorgen Ilstad, Wahida Gasti, Peter Sinander, Sandi Habinc, "SpaceWire Remote Terminal Controller", International SpaceWire Conference 2007, Dundee (Scotland), 17-19 September 2007
2. Sandi Habinc, Tom Seeman, Jiri Gaisler, "Remote Terminal Controller Based on LEON2-FT and GRLIB", DAta Systems In Aerospace 2006, Berlin (Germany), 22–25 May 2006
3. ARM Limited, "AMBA™ Specification", 13 May 1999
4. SPARC International Inc., "The SPARC Architecture Manual - Version 8", 1992
5. Gaisler Research, "GRLIB IP Library User's Manual", 2006
6. Gaisler Research, "GRLIB IP Core User's Manual", 2006
7. Gaisler Research, "The LEON2-FT Processor User's Manual", 13 February 2007
8. Gaisler Research, "TSIM2 Simulator User's Manual", May 2007
9. Gaisler Research, "GRMON User's Manual", January 2007
10. Gaisler Research, "GRESB Ethernet/SpaceWire Bridge", August 2007
11. Gaisler Research, "RCC User's Manual", April 2006
12. Gaisler Research, "VxWorks 5.4 LEON BSP", September 2006