SPACE CUBE 2 - AN ONBOARD COMPUTER BASED ON SPACE CUBE ARCHITECTURE

Session: SpaceWire onboard equipment and software

Short Paper

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ABSTRACT

Space Cube 2 is a space-wire based onboard computer designed for future science missions in Japan. It has been developed as a successor of Space Cube 1, which is the commercial version of a minimum set of on board computer to be used on the ground. The combination of Space Cube on the ground and Space Cube 2 in space provides us with a user-friendly platform for the developments of satellites, since one could develop onboard software and flight equipments with low-cost commercial Space Cube and then easily integrate these Space-Cube2 based satellites .

INTRODUCTION

Scientific satellites often require different specifications of how the components are linked and controlled. The size and transmission speed between scientific instruments and data processors are also different from each other. Flexibility is thus the key when we investigate an architecture which can be used for a variety of scientific missions. Another issue is that mission components are often designed, built and tested by university members distributed in various places. Therefore, we need to have clearly-defined interface between the components and the bus system. Additionally, we need to prepare an easy-to-use (and inexpensive) ground support system to members, such

that most of the functionality tests including the interface can be done in the universities prior to integration.

In order to develop spacecrafts in a short time without losing reliability, Space Wire is an attractive standard. The standard interconnection between modules in both hardware and protocol levels is important to realize a system which can be easily tested. The Remote Memory Access Protocol (RMAP) for Space Wire provides a standard method for reading and writing to registers and memory among mission- and bus- components, leading to further standardization by introducing the abstraction of the access method to individual components. Once a set of middle ware is prepared based on the RMAP access, the time to write applications could be reduced significantly even with different implementations of the hardware. Another merit of the Space Wire standard is its simplicity. The logic can be readily implemented in Field Programmable Gate Arrays (FPGAs).

NET WORK BASED ARCHITECTURE AND "SPACE CUBE 1"

We have adopted the Space Wire standard for a series of small scientific satellites organized at ISAS/JAXA after some experiences in designing medium-size science missions, such as MMO (Bepi Colombo) and NeXT (X-ray astronomy) [1]. Space Wire enables us to define distributed system with a network topology. Figure 1 shows a diagram of the possible architecture to be adopted in future scientific satellites in Japan. Based on the interconnection via Space Wire, this concept could realize the modular structure and the scalability of the system and promote the re-use of resources. To make such an environment in real spacecraft, we need to prepare a standard computer for both on the ground and in space, as well as space qualified LSIs for the router and the SpW interface to be mounted in sensors and actuators.

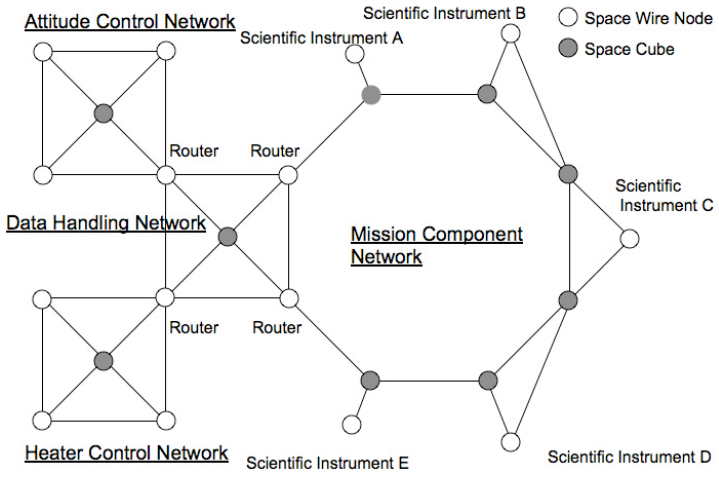

Figure 1. Architecture of the future distributed system based on Space Wire

Since the initial phase of the project, we have developed various kinds of sensor electronics with the Space Wire interface for ground-based and balloon-borne experiments [2]. Space Cube 1 was developed to control these electronics in collaboration with ISAS/JAXA and Shimafuji Electric[1]. Space Cube 1 features and

[1] Shimafuji Electric Incorporated, 8-1-15 Nishikamata, Ota, Tokyo, Japan 144-0051

various I/O interfaces include three channels of Space Wire interface with logics implemented in FPGAs, inside a very compact size, 52 x 52 x 55 mm. It includes 16 MB of Flash memory, along with audio, and a D-sub RS232 serial port. The board also offers a D-sub 15 video port. In order to have high throughput in data acquisition, Space Cube 1 uses the latest version of the TRON real time operating system, which is called the "T-Kernel"[2]. After having applied Space Cube 1 to various projects, we have learned that this kind of "standard computer" is very useful to help simulate network-based distributed systems with multiple Space Wire nodes.

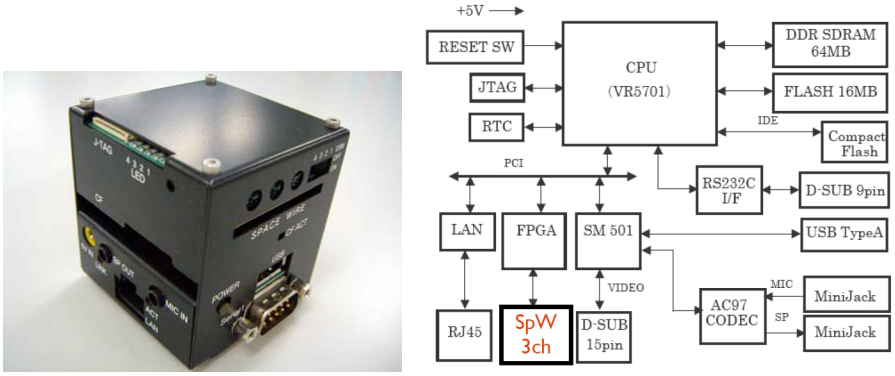

Figure 2 Photo of Space Cube 1 and the block diagram

"SPACE CUBE 2" COMPUTER

Space Cube 2 is a generic multi-mission platform developed by JAXA/ISAS and NTSpace in 2005 for space application. Space Cube 2 is based on the concept of Space Cube 1 and integrates in a single modular stack. The block diagram of Space Cube 2 is shown in Figure 2.It consists of three modules, the CPU, a Data Recorder and Power Supply modules. HR5000, which has been developed by JAXA, is the central processor chip of the system. The chip contains 64bit micro-controller based on MIPS 5kf architecture with maximum clock speed of 200 MHz With integrated peripheral devices the chip enables high-speed communication and control. The specifications of Space Cube 2 are summarized in Table. 1. We operate the CPU at 33 MHz to reduce the power. We use bus connectors to fabricate the stack structure to eliminate back planes. Furthermore, it is possible to add user modules as long as they meet the requirements of the stack module interface, mechanically, thermally and electronically. The first demonstration of Space Cube 2 (Figure 3) in space will take place in 2008 by using JAXA's technology demonstration satellite, SDS-1. In this mission, we will use Space Cube 2 as a data acquisition computer for user modules that measure acceleration of free-falling test masses.

Further developments to promote the Space Wire standard are on going. The activities include a router LSI with 15 port Space Wire and one PCI interface by using the cross bar switch technology. A small-scale Space Wire chip with simple parallel bus interface and DMA capability will also be prepared, this year.

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[2] Space Cube 1 also supports Linux.

Figure 3 Space Cube 2

Table 1 Specifications of Space Cube2

CPU	HR5000 (33 MHz)
Space Wire Interface	3 ch (additional ports available)
System Memory	2 MB Flash Memory 4 MB Burst SRAM
	4 MB Asynchronus SRAM
Data Recorder Memory	1GB SDRAM 1GB Flash Memory
Size (mm)	71（W) x 220.5 (D) x 170.5 (H)
Weight	1.9 kg
Power Consumption	7 W

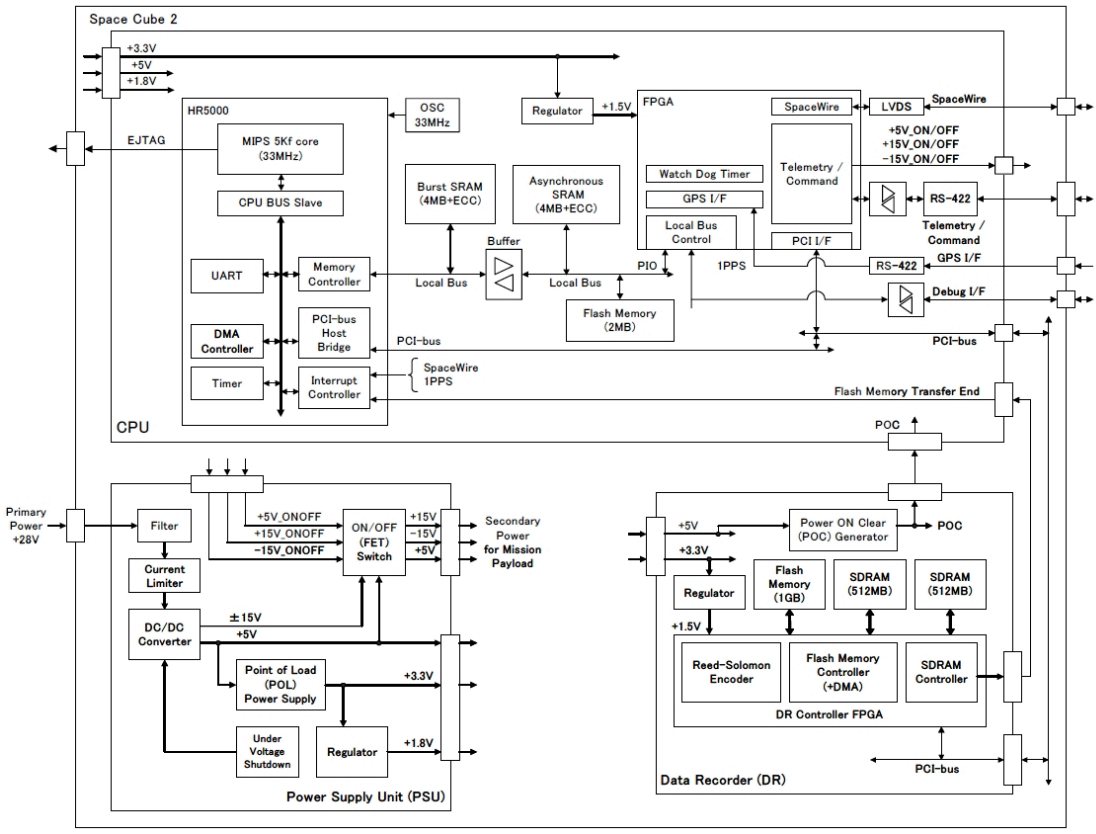

Figure 4 Block diagram of Space Cube 2

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