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GRSPW SpaceWire Codec IP Core and its Application

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Enabling technologies

The following enabling technologies allow the development of advanced System-on-a-Chip designs for on-board application at an unprecedented rate:

- SPARC 32-bit RISC Architecture:
  - standardized instruction set portable between processor generations: e.g. ERC32, LEON2/3/4
- Debug Support Unit:
  - instruction and on-chip bus tracing
  - Debug Link UART: remote read/write
- AMBA AHB/APB on-chip bus
- SpaceWire link with RMAP

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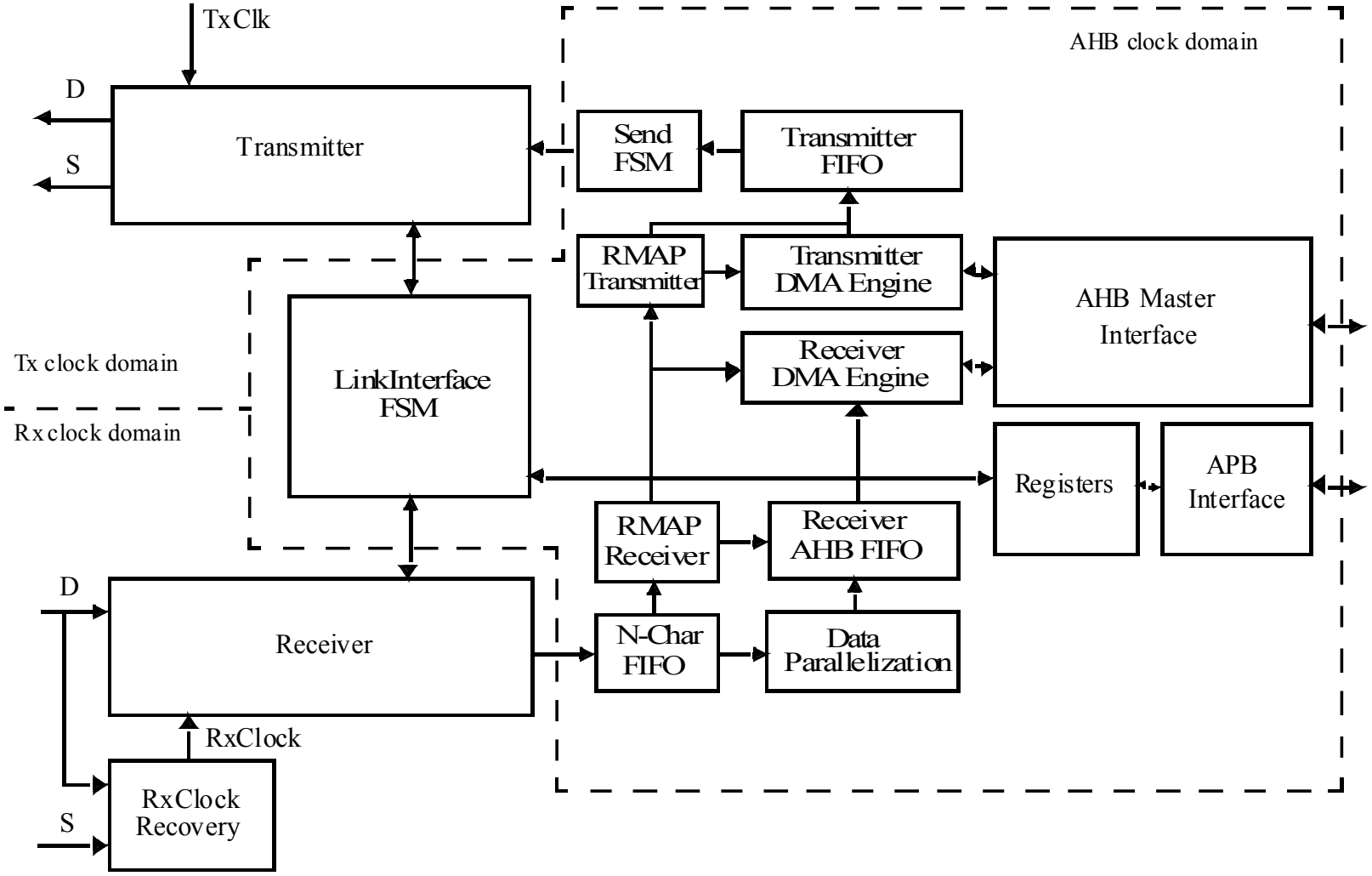
AMBA On-chip bus

Key features of the Advanced Microcontroller Bus Architecture (AMBA):

- Fully pipelined arbitration phase, address phase and data phase
- Multi-master, multi-slave
- Burst access: incremental or fixed size (up to 1024 bytes)
- Byte, half-word, word or larger data structures (up to 1024 bits)
- Separate high-performance and peripheral buses
- Open, non-licensed, standard
- Extended with plug&play

The standardization has resulted in a multitude of synthesizable cores that are integrated in system-on-a-chip designs.

GRSPW Codec

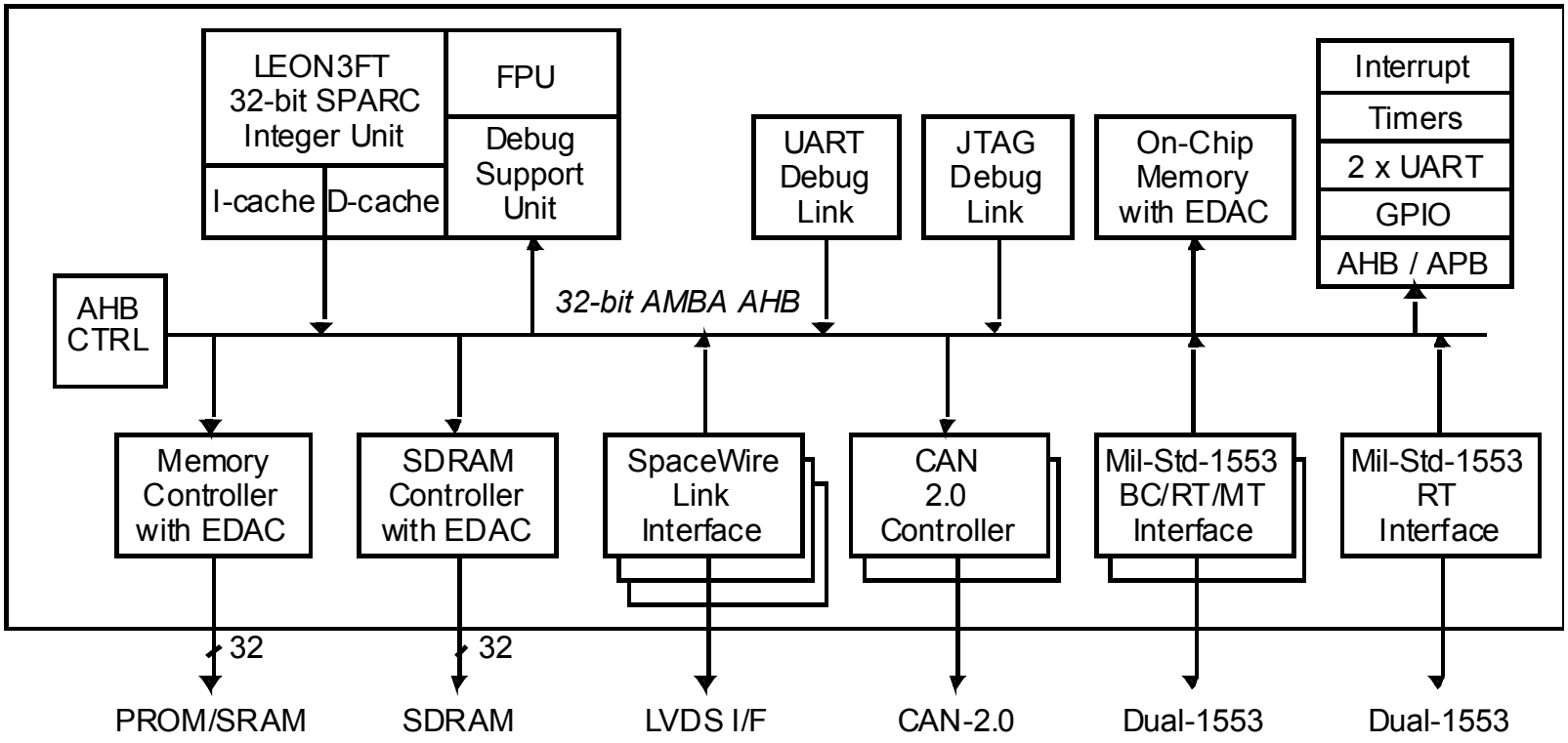

TxClk
AHB clock domain
D
S
Transmitter
Send FSM
Transmitter FIFO
RMAP Transmitter
Transmitter DMA Engine
AHB Master Interface
Tx clock domain
Rx clock domain
LinkInterface FSM
Receiver DMA Engine
Registers
APB Interface
RMAP Receiver
Receiver AHB FIFO
D
Receiver
N-Char FIFO
Data Parallelization
RxClock
RxClock Recovery
S

GRSPW - Characteristics

- Supports AMBA AHB with high throughput
- Supports full RMAP
- Fault-tolerant version /w memory protection
- Portable between technologies and tools: Xilinx, Actel and ASIC
- Small footprint on Actel (Companion Core)
- RTEMS and VxWorks drivers available

Core configuration	RTAX2000S-1	ASIC
GRSPW	2,800 / 2 / 40 / 100	10,000 gates
GRSPW + RMAP	3,600 / 2 / 40 / 100	15,000 gates
GRSPW-FT	2,900 / 4 / 40 / 100	11,000 gates
GRSPW-FT + RMAP	3,700 / 4 / 40 / 100	16,000 gates

LEON3-FT-RTAX, Actel RTAX2000S



Actel RTAX-2000S CCGA-624 or CQFP-352

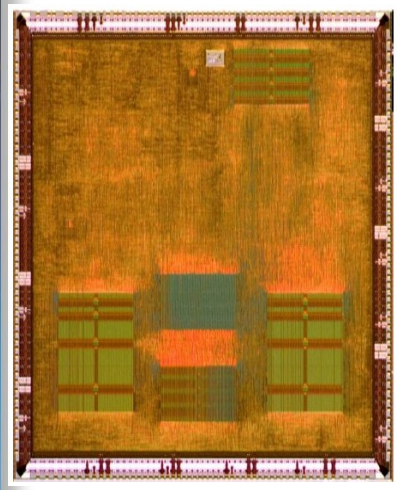
20-25 MHz system frequency, up to 100 MBPS SpaceWire

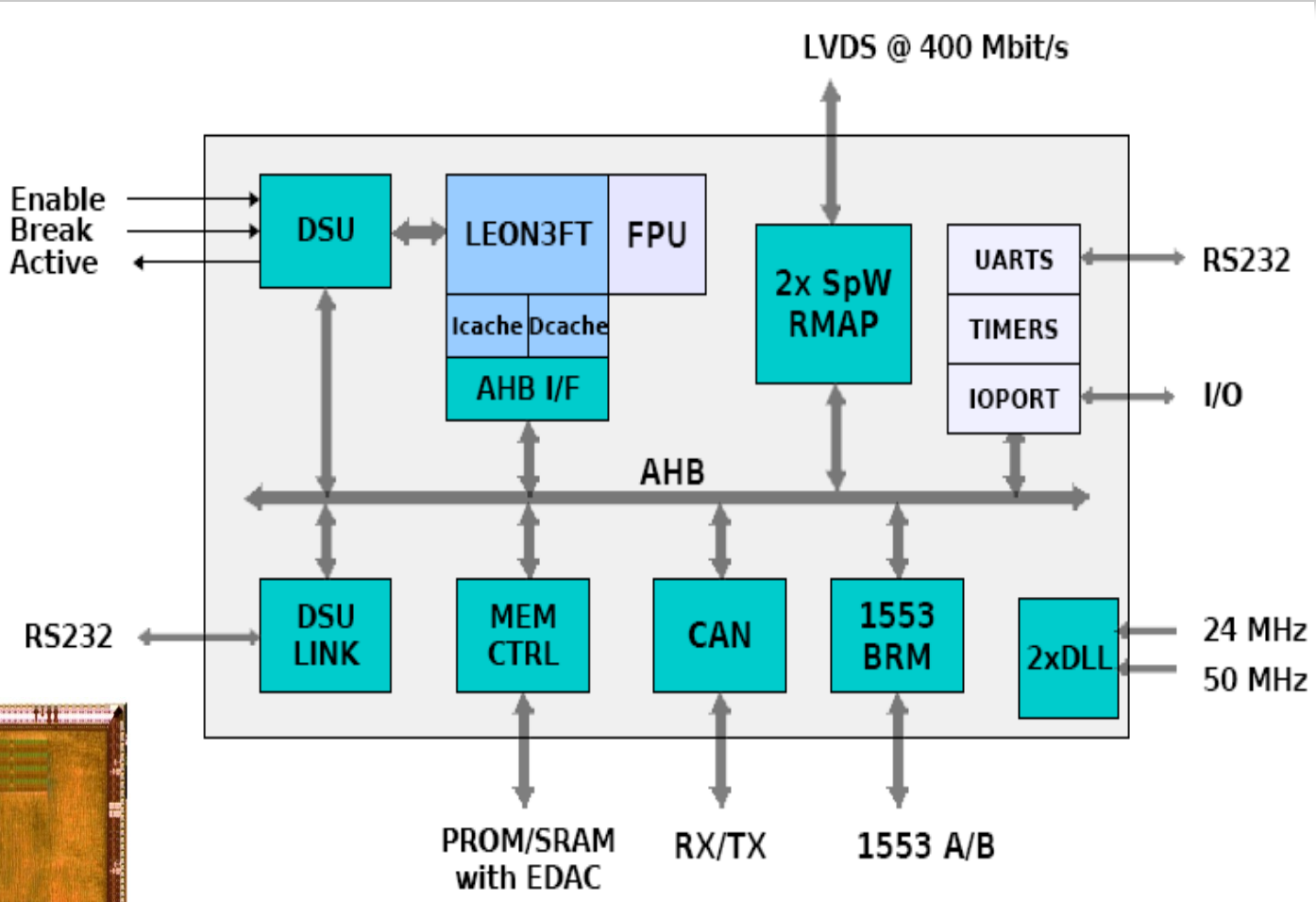
Several systems already shipped

Delivered as programmed component or as individual IP core netlists

Supports Actel Libero design flow

LEON3-FT GR702RC



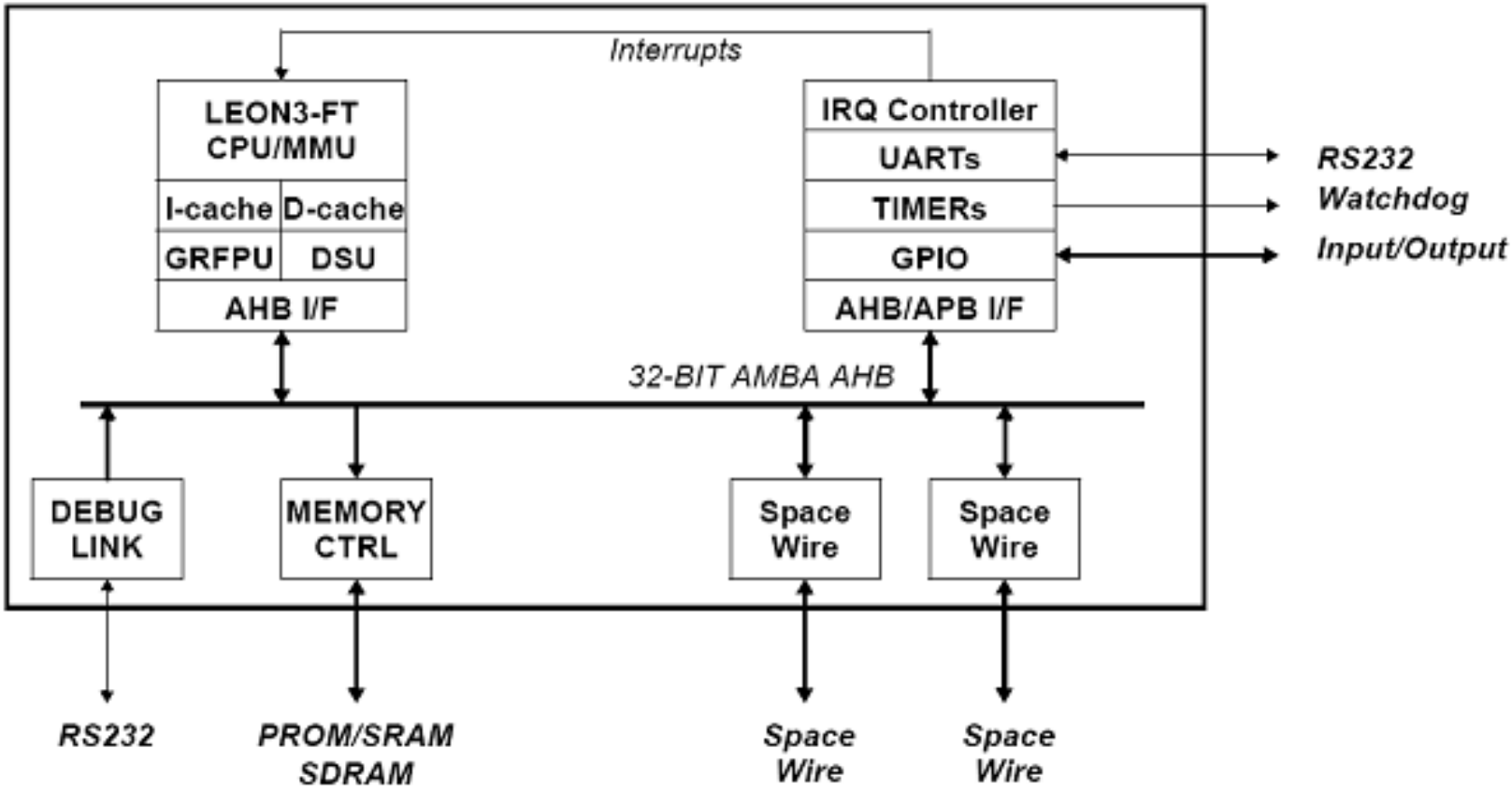


Tower 180 nm technology, Ramon Chips rad-hard library

Fully functional up to 125 MHz, 10 mW/MHz

Successfully validated under radiation [see DASIA 2007]

LEON3-FT DARE

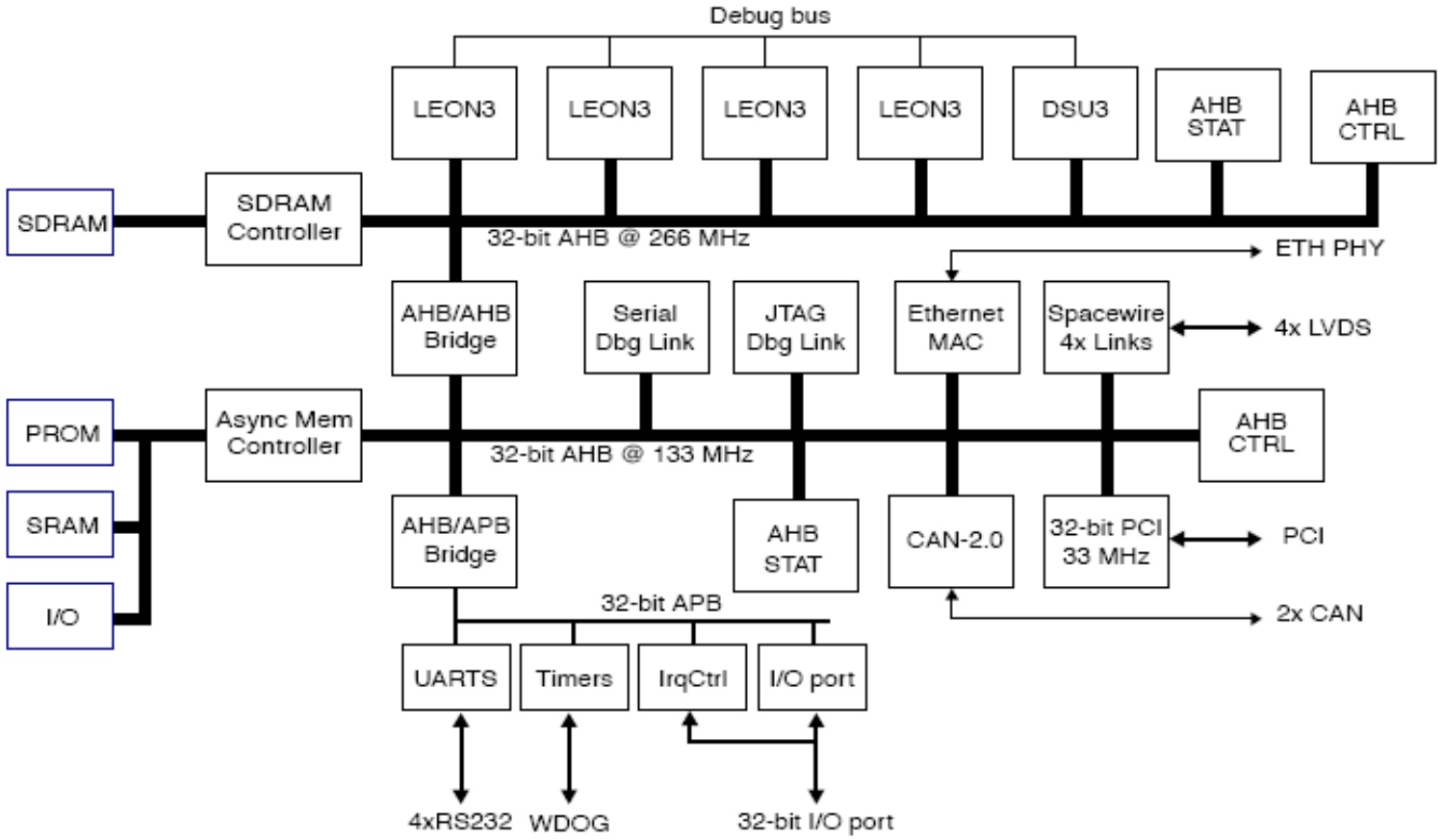


ESA activity with the aim to implement and characterize the complex ASIC on radiation-hard UMC 180 nm technology (DARE)

ADR passed in September 2007, device in 3Q2008

Target operating frequency of 100 MHz and 200 MBPS SpaceWire

LEON3-FT–MP (GINA)



ESA activity with the aim to implement multi-core processing

ST 90 nm technology as baseline

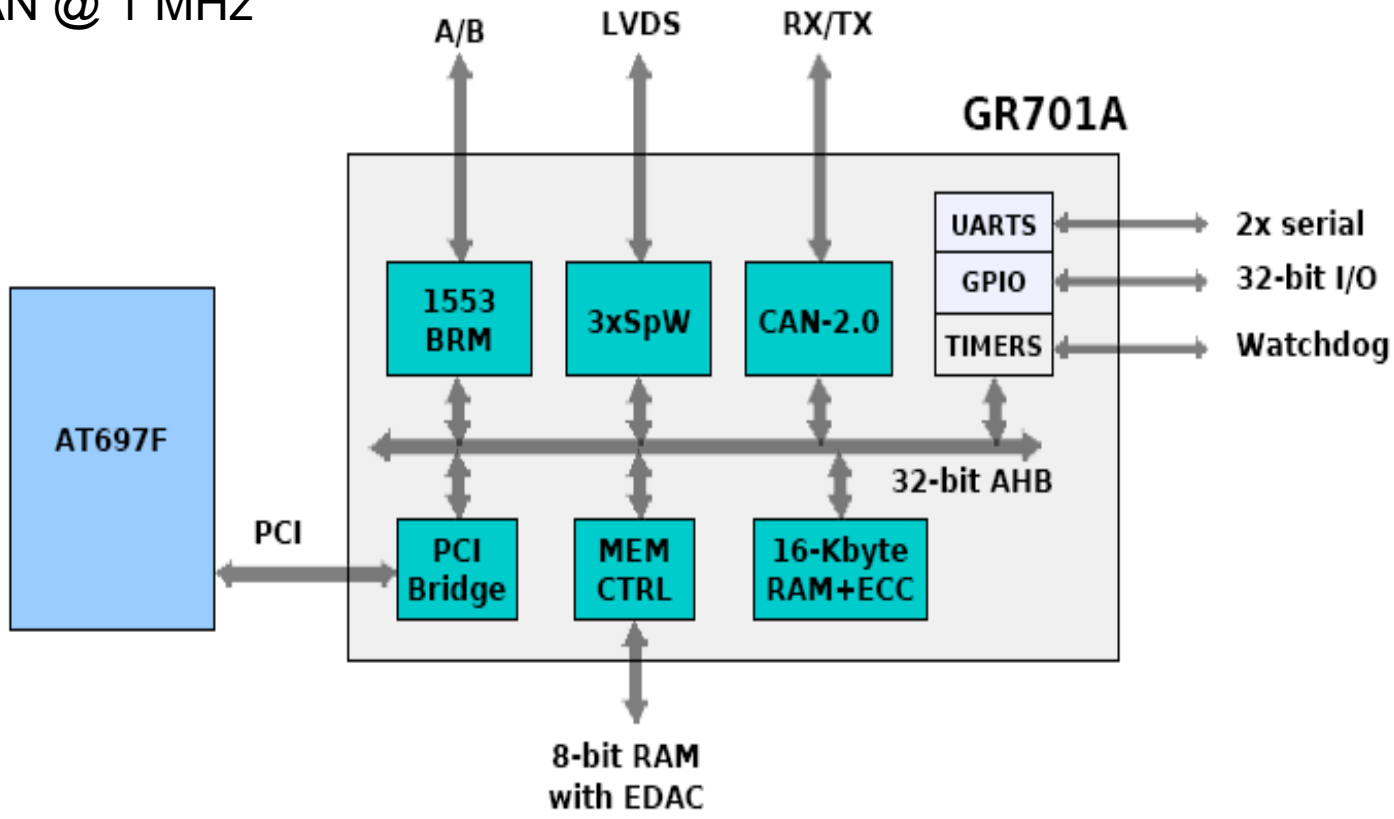
Tape out planned 2008

Target performance of 1 GIPS / 1 GOPS and 200 MBPS SpaceWire

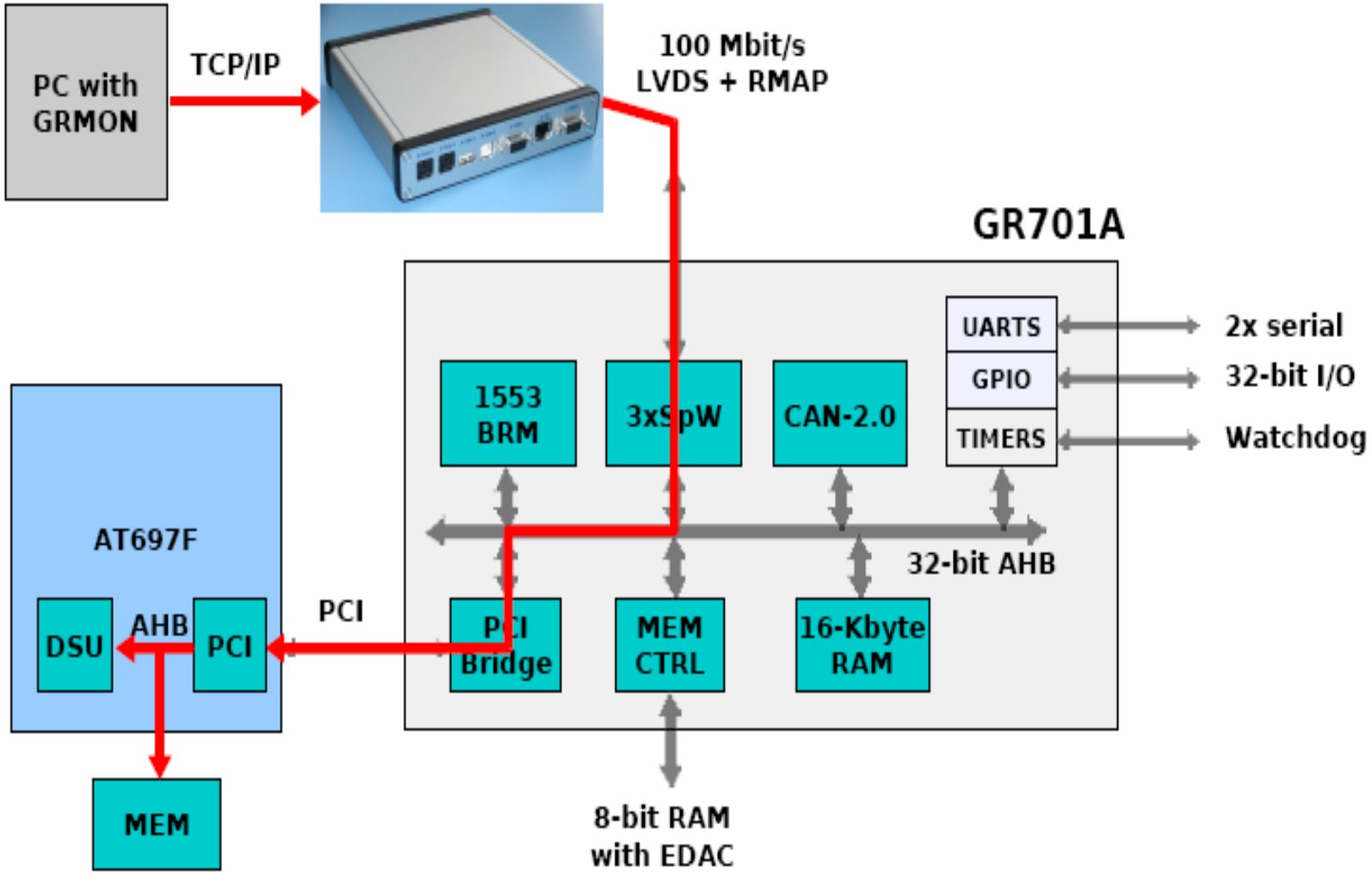
GR701 - Companion Chip

PCI based companion chip implemented on RTAX2000S FPGA:

- PCI @ 33 MHz (Actel)
- 1553 @ 24 MHz (Actel)
- SpaceWire @ 100 MHz
- CAN @ 1 MHz

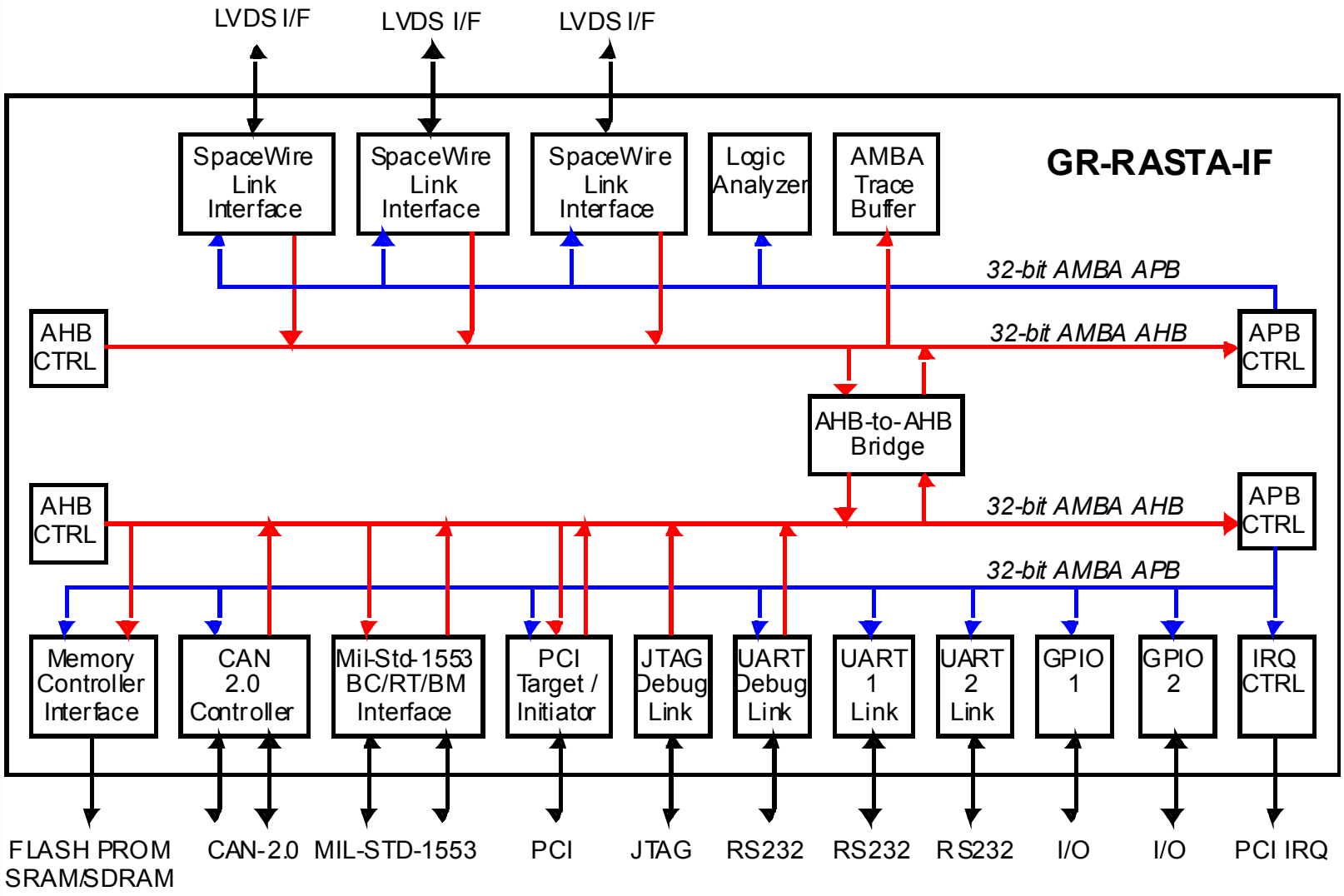


Debugging with GR701

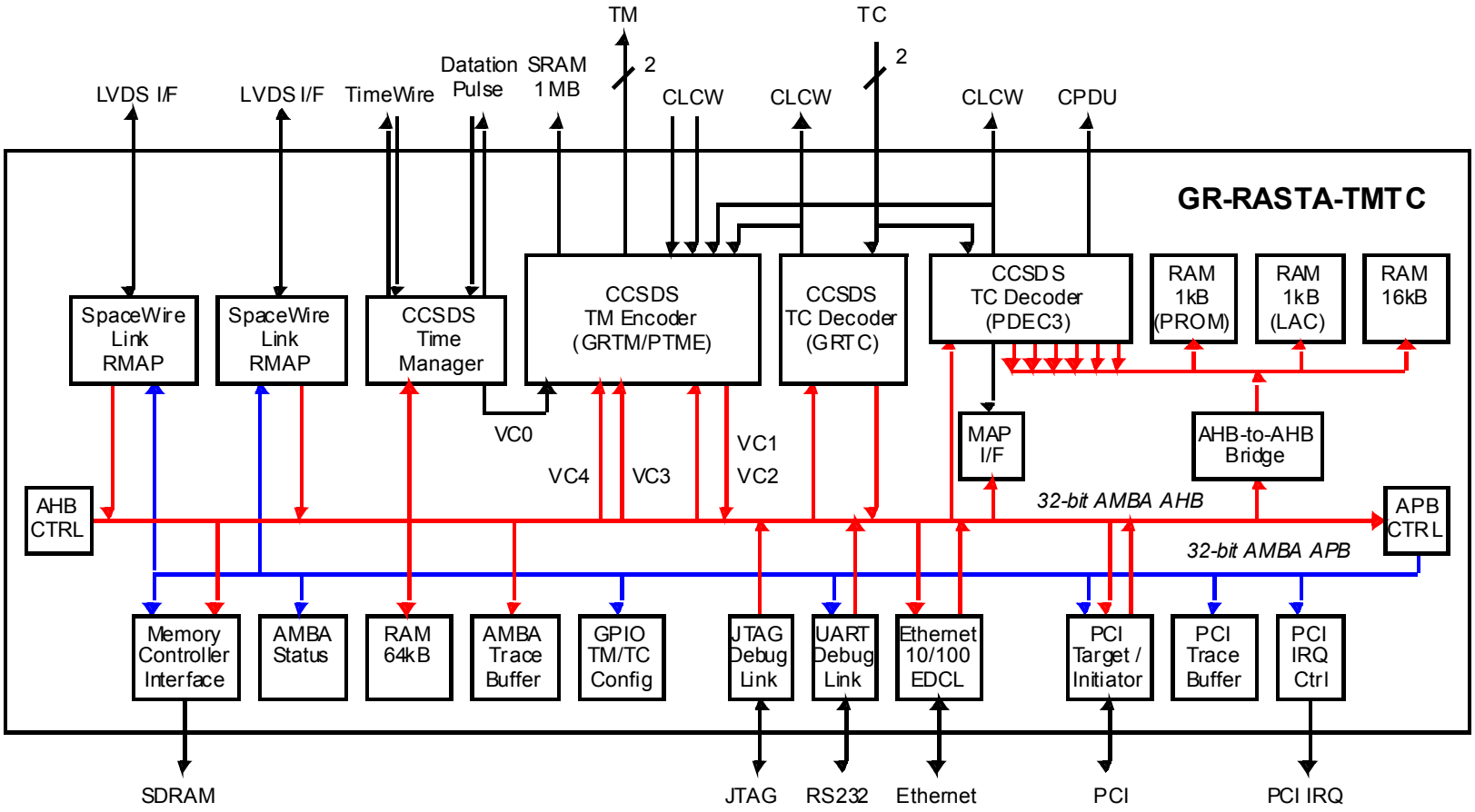


GR-RASTA CPCI Crate

RASTA Interface Board



RASTA TM/TC Board



Conclusion

By embracing the enabling technologies presented, several powerful system-on-a-chip designs have been developed in a short period of time.

The key factors have been efficient implementation of truly re-usable IP cores, such as the GRSPW SpaceWire codec, which have been designed with interoperability and portability in mind from the start.

This has resulted in sophisticated flight products that are being shipped to customers right now.