Spacewire cabling in an Operationally Responsive Space Environment

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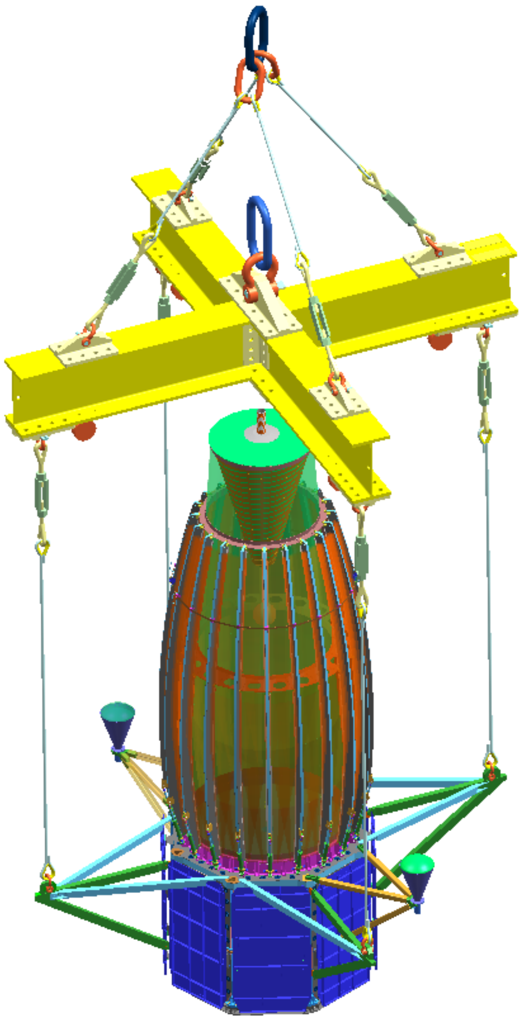
Agenda

- Introduction
  - What is ORS?
  - What's a depot?
- Problem
  - Connectors
- TacSat-4 SpaceWire
  - Cabling design
  - Qualification testing plan
- Results
  - Differential impedance
  - Time domain waveforms
  - BERT testing
- Summary
- Backup Slides

What is ORS?

- ORS stands for Operationally Responsive Space.
- The aim is to make space assets more accessible to the commanders in the field.
  - ORS satellites can be considered “the UAVs of Space”.
- The vision is call-up to launch in less than seven days.
- This vision requires having inventory of space assets ready.
  - Use pre-built busses and payloads
    - Mix and match
    - Stored in a depot
    - Upon call up, mate bus to payload, then stack and launch
  - Want to leverage/enable Industry for cost savings
    - Any manufacturer can build a bus or payload
    - Will not be build to point design, is build to requirements
- The satellites in question are small, nominally < 500 kg.
- TacSat (tactical satellite) experiments are part of the ORS effort.

Depot Concept



Mission specific Payload

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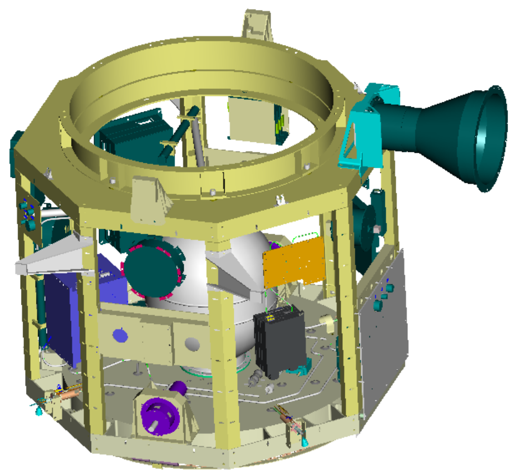

"Off the shelf" Generic ORS bus

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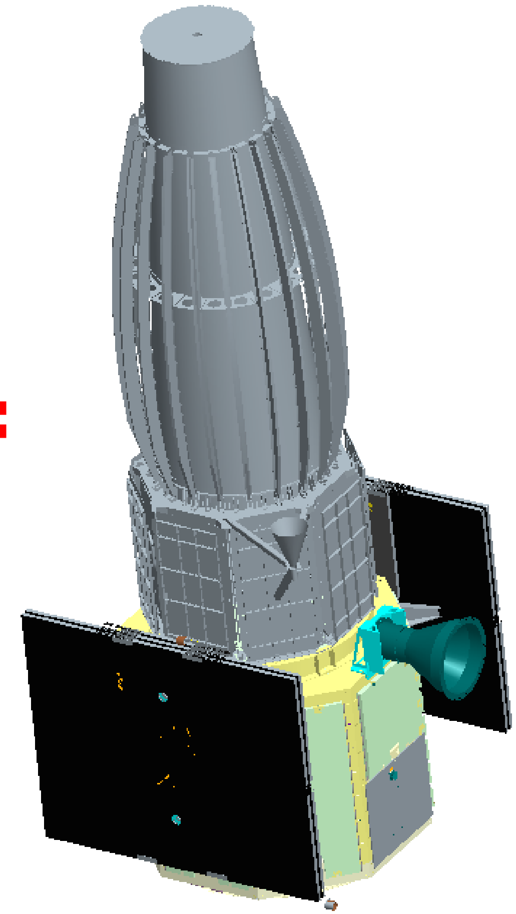


Integrated SV

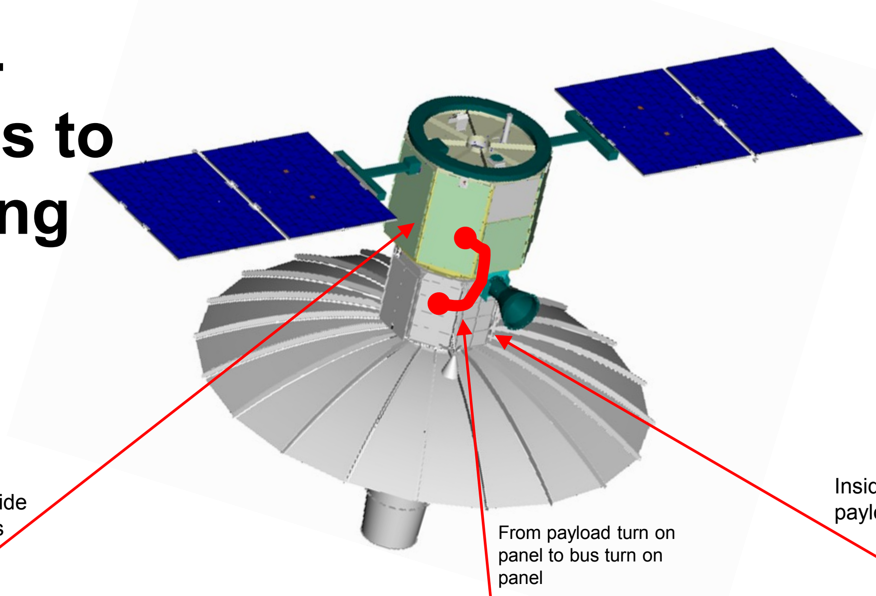
Operationally Responsive Space Requirements for Spacewire Connectors

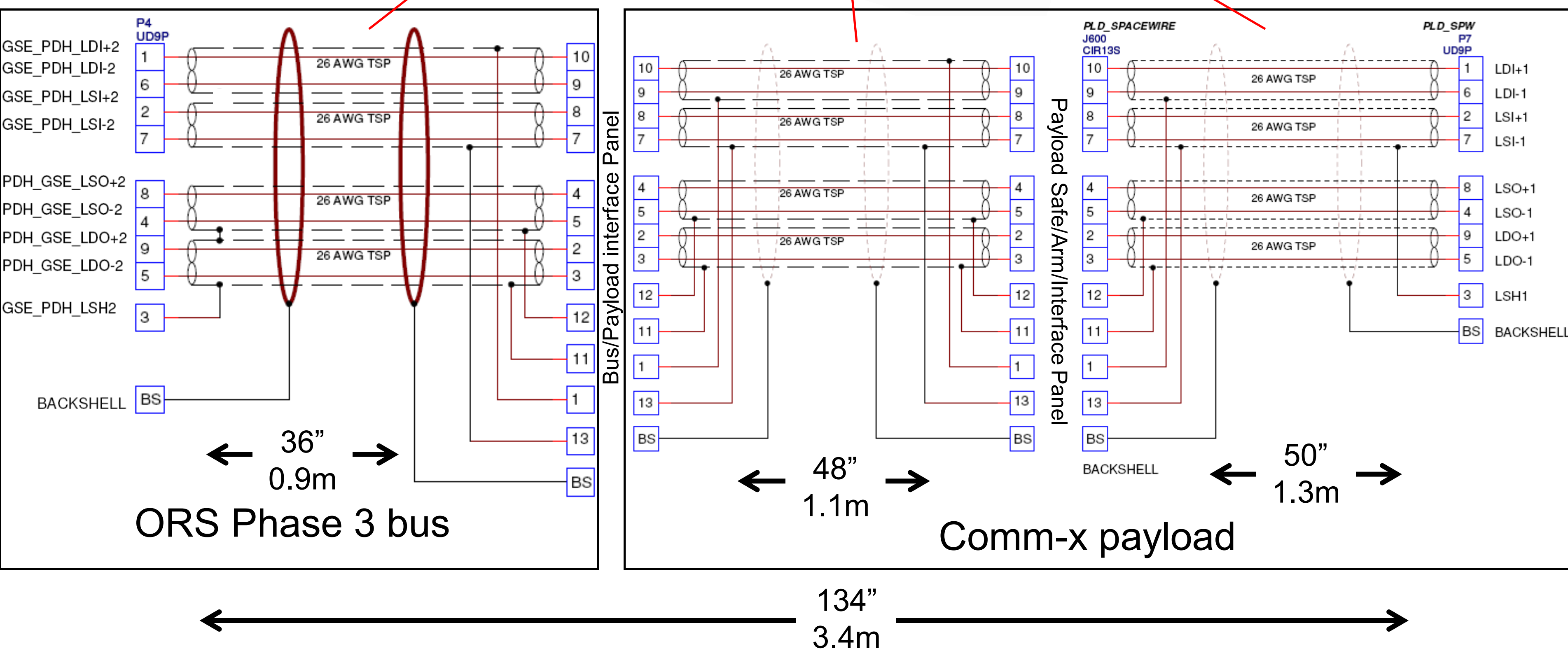
- Suitable for Space Applications
- Signal Integrity and Impedance control
  - Ability to reliably support Spacewire
- Availability
  - Should be fairly widely available
- Cost
  - Should not be exorbitantly expensive
- Suitable for Depot Operations
  - Quick, reliable connection
  - Usable by minimally trained personnel
  - No torque requirements
  - No need for tools

Connectors Considered

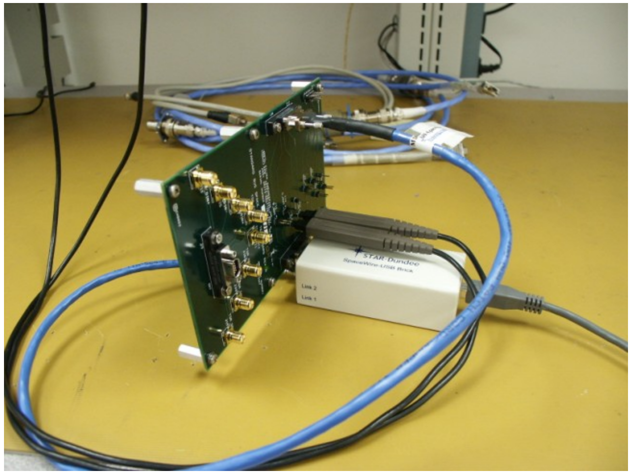
	Cost	Lead Time	Availability	Depot Assembly	Impedance Control	EMI Control
D connector	Low	Short	High	Fairly easy	Low	Low
High density D	Low	Short	High	Fairly easy	Low	Low
Micro D	Med	Long	Low	Tricky	Low	Low
Gore JWST twinax	High	Long	Low	Fairly easy	Very good	Very good
38999	Med	Med	Med	Simple	Med	Med

TACSAT-4 SpaceWire bus to payload wiring



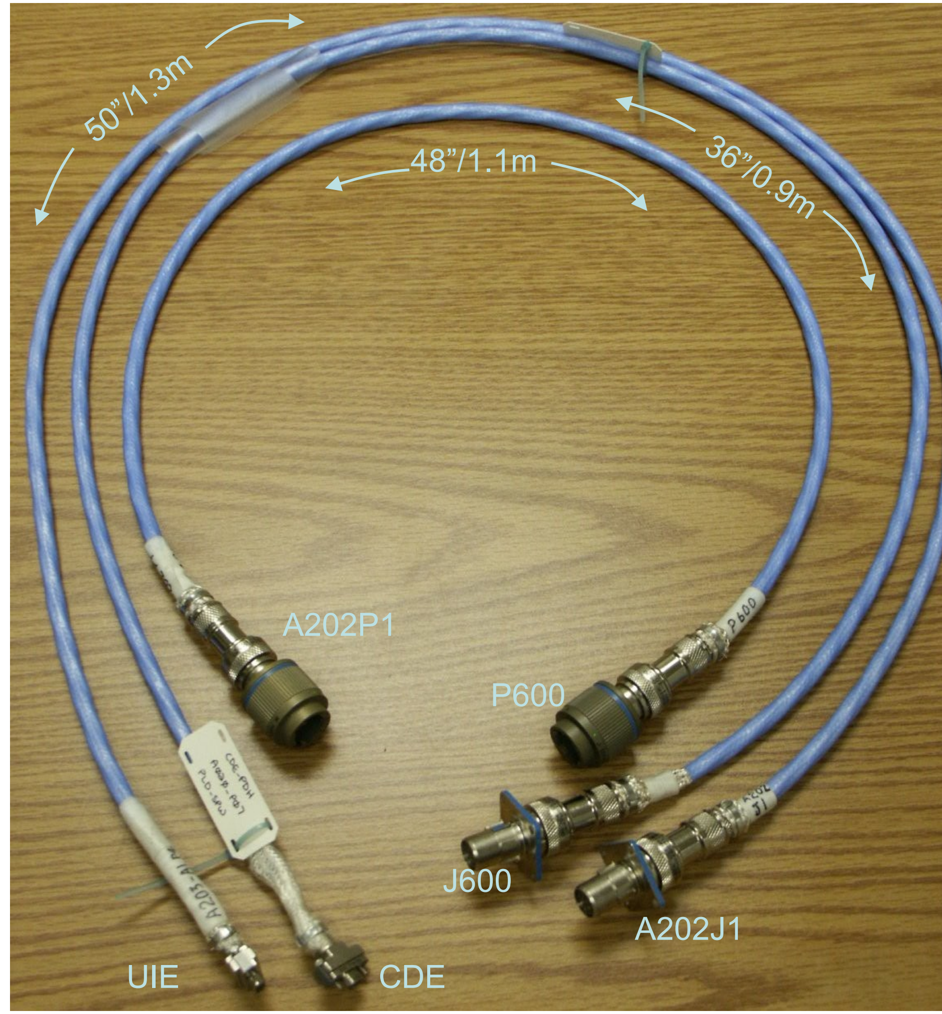


Test Cable Images



Blue reference cable, test board and SpaceWire brick in waveform capture configuration

DVI – heritage Reference cable

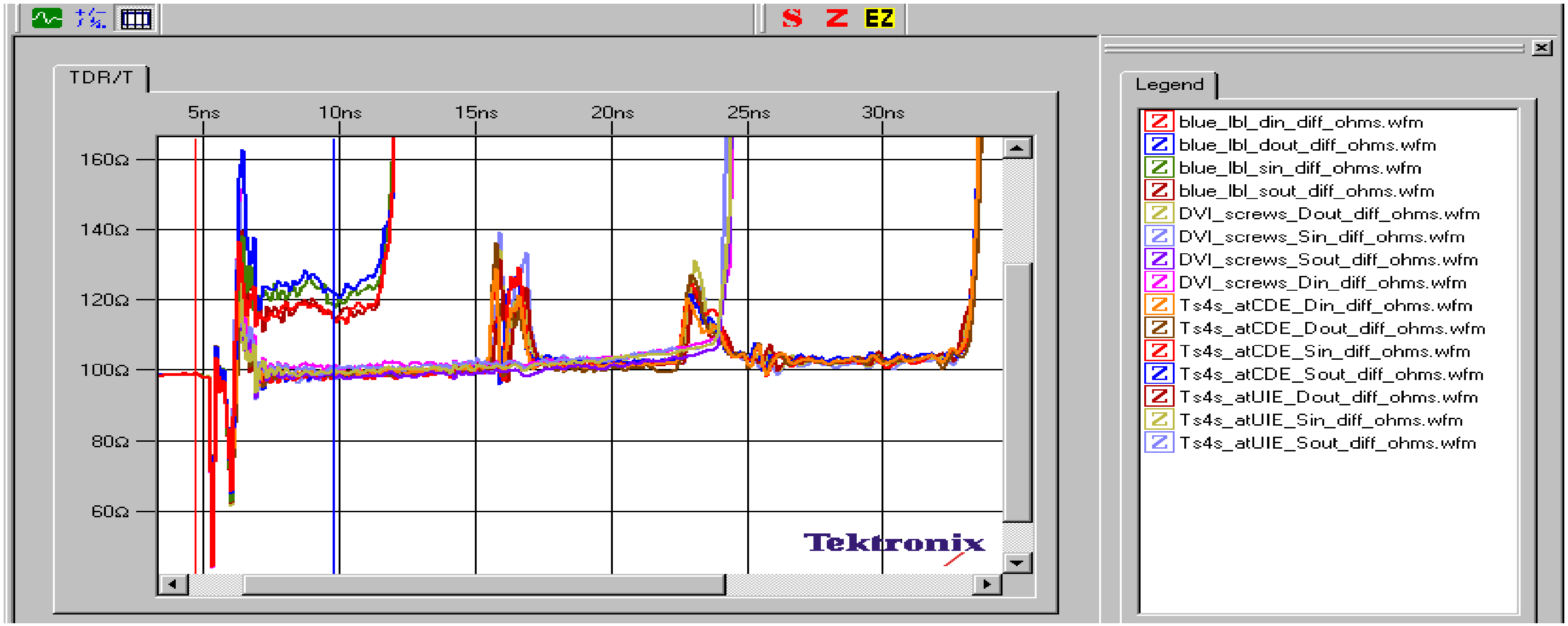


Tacsat-4 flight spacewire cable (unmated)

Tacsat-4 / NRL's SpaceWire Testing (To date)

- Tests were baselined against a COTS 3m (DVI-heritage) cable and a 0.5m cable from Dynamic Engineering
- Testing includes:
  - compare v. baseline
  - Differential Impedance
    - Via TDR
  - Limited scope traces
  - Data rate tests
- Data rate testing done with the STAR-Dundee SpaceWire/USB brick
  - In loopback mode (with and without test board inline)
- Test cables were hand fabricated by NRL's harness group.
  - Used the TacSat-4 flight cables
  - Segment lengths as shown above (3.4m, total)
  - Pinout chosen by graphically using "ORS Spacewire Connector (10-35P) conductor configuration" slide in this presentation
    - Attempted to make conductor configuration for each pair as uniform as possible
    - Attempted to align **E** and **H** fields
- Test was performed at max speed for driver (136Mbs)
- All scope probing was done on a Tex TDS644A with a Tex P6246 *400MHz* diff probe.
  - Input Capacitance <1pF
  - Input resistance ~200kΩ
- TDR Testing was done on a Tektronix DSA8200 with a 80E04 differential TDR head
  - Impedance correction done in Iconnect (80SICMX)
- A spacewire test board (test fixture) was fabricated to facilitate easier testing

Testing Results (Cable, Impedance)

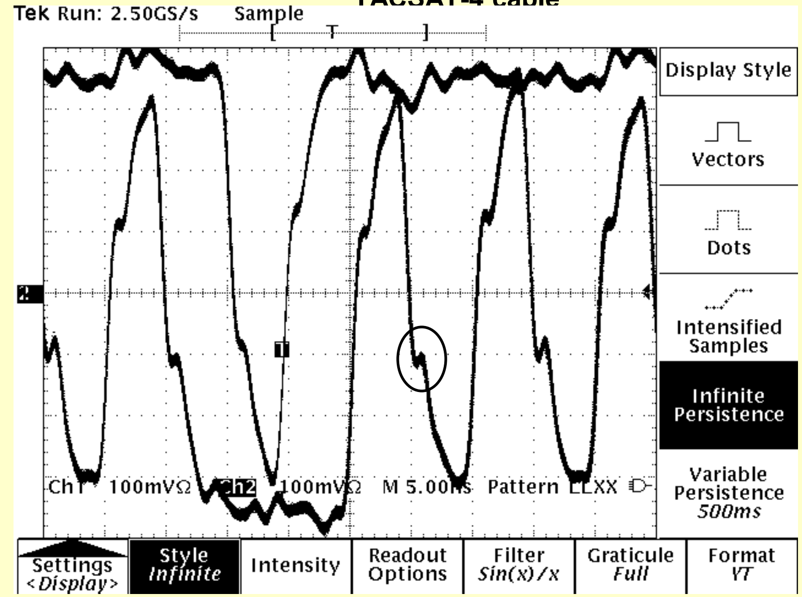


- Conclusions
  - Blue test cable is not 100Ω! It is 120Ω.
  - Grey/DVI Ref cable and TacSat-4 cables are a very consistent 100Ω
  - The ORS 38999 Series II connector creates an impedance discontinuity of up to 40Ω for 2ns.
  - The asymmetric impedance of the connector is less severe than in previous studies.
    - Because of cable layout, these traces go through the first connector pin to socket, then socket to pin through the second (and vice versa).
    - There is not a significant difference between traces taken from CDE or UIE end of cable.
    - There is a difference between the first connector and second.
      - Most likely due to loss of TDR resolution after the first discontinuity (from previous TDR experience)
      - This raises concerns about the discontinuities from the SMA, test board and first uD connector
      - When evaluating this connector, its best to look at the first instance of it in the above TDR traces.

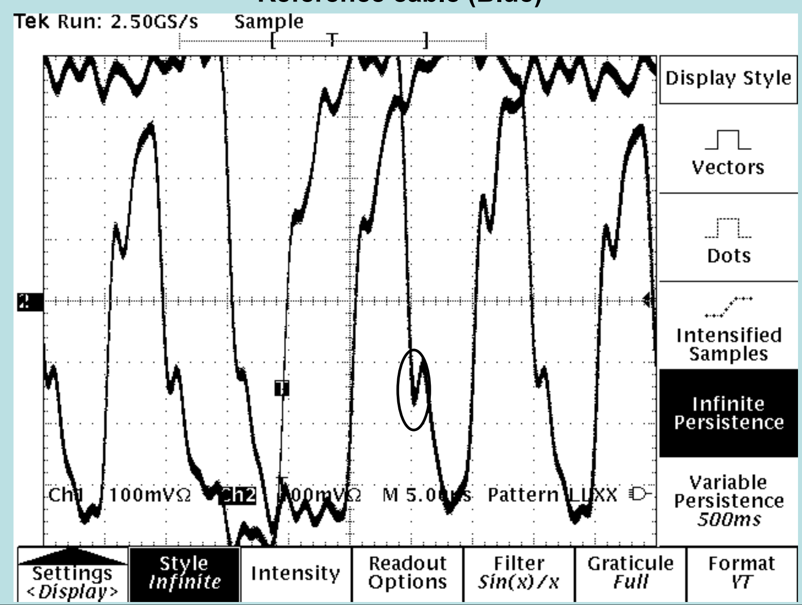
Testing Results (scope)

- Conclusions
  - Both cables run error-free at 136MHz with the spacewire brick in loopback mode
    - Adding/removing the test board doesn't affect link speed –except gray DVI cable
  - Scope traces look almost identical
- Issues/Concerns
  - Non-monotonic leading edge (in circle)
    - Is on both traces, so is probably from the test set-up
  - These traces were captured with a 500MHz scope using 400MHz probes…doubtful that was enough bandwidth.
  - Why didn't the grey cable work?
- Recommendations
  - Previous testing at 61Mbs showed the same results, so the following are not expected to be a significantly different, but should be done for closure:
    - 1GHz probes and scope are on order, retake images with them
    - Work with Dundee to get the brick running at 200Mbs and retake the images
  - Why no difference?
    - Because signal spectral content is related mostly to rising edge and the driver produces the same edge rate at 61Mbs as it does at 136 or 200.
  - What would make a difference?
    - Should compare eye diagrams of these cables

TACSAT-4 cable



Reference cable (Blue)



Summary

- TacSat-4's SpaceWire cable assembly is qualified to at least 100Mb/s
  - More testing might qualify it to 200Mb/s or faster operation
- Future SpaceWire Cable qualification recommendations:
  - compare v. baseline
    - Differential Impedance via TDR
    - Cross-talk, jitter and skew analysis (addition)
    - Limited scope traces
      - Add eye diagrams (add)
      - Standard time domain waveforms
    - Data rate and data compare tests
  - Perform at max speed for driver (200Mb/s?)
  - All scope probing on a >1GHz scope and probes
- Further work
  - As noted rerun scope, loopback tests at 200Mb/s with >1GHz scope and probes
  - Take eye diagrams, perform cross-talk, jitter and skew analysis

Backup slides

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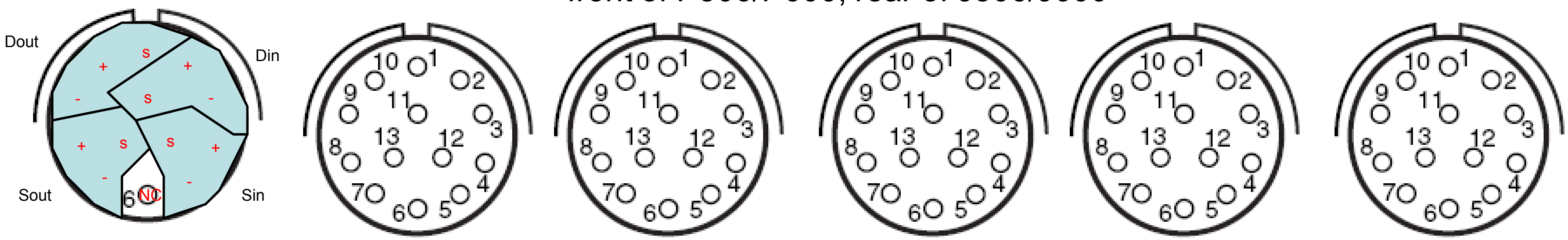
TacSat-4 Spacewire Implementation Notes

- Spacewire “driver” is Payload Data Handler designed by Greg Clifford, of SEI
  - Partial heritage to SECCHI design
  - Details available from Greg Clifford (gclifford@silvereng.com) or via ORS Phase III Bus CDR material
- Spacewire “receiver” is UIE
  - Details TBR
  - Spacewire experiment is a Payload distinct from comm-x
- Interconnect configuration:
  - 38999 Series II (10-35 conductor configuration) 13-pos Circular connector:
    - D38999/40FB35SN (447HS166M11-10-4 backshell) for the bulkhead connector (J506/J600)
    - D38999/46FB35PN (same backshell) for the payload-side cable (P506/P600)
    - 22 ga contact.
    - 4-8wk lead time to get exact connector
  - Our harness group built the spacewire cable assemblies Gore-Tex 26AWG (GSC-05-82730-00) space wire cable (W. L. Gore & Associates GmbH)
  - 3 segment cable (as above) with a total length 3.4m
    - CDE to interface panel
    - I/F panel to intermediate payload panel
      - payload intermediate i/f also a 38999 series II
    - Intermediate payload panel to payload Spwr load.
- One path from CDE to Payload (as noted above)
- One path from CDE to EGSE (debug port)
  - Two segment in ambient testing
  - Three segment in TVAC

ORS Spacewire Connector (10-35P) conductor configuration

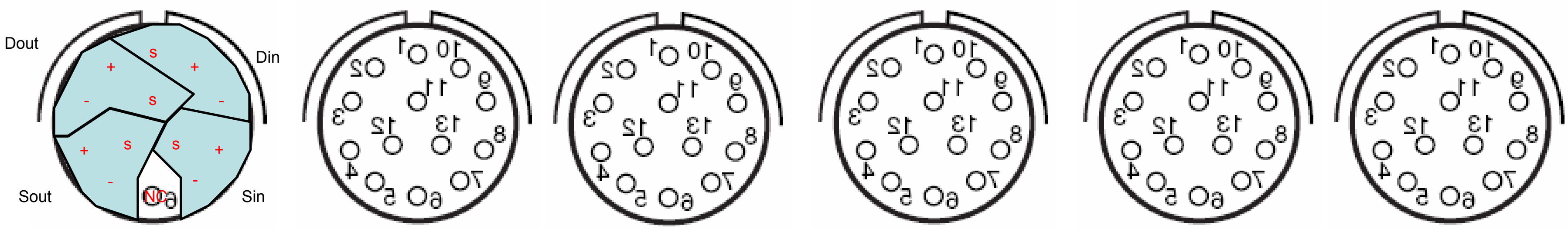
Bus to payload (@J506/J600)

front of P506/P600, rear of J506/J600



Payload to bus (@J506/J600)

rear of P506/P600, front of J506/J600



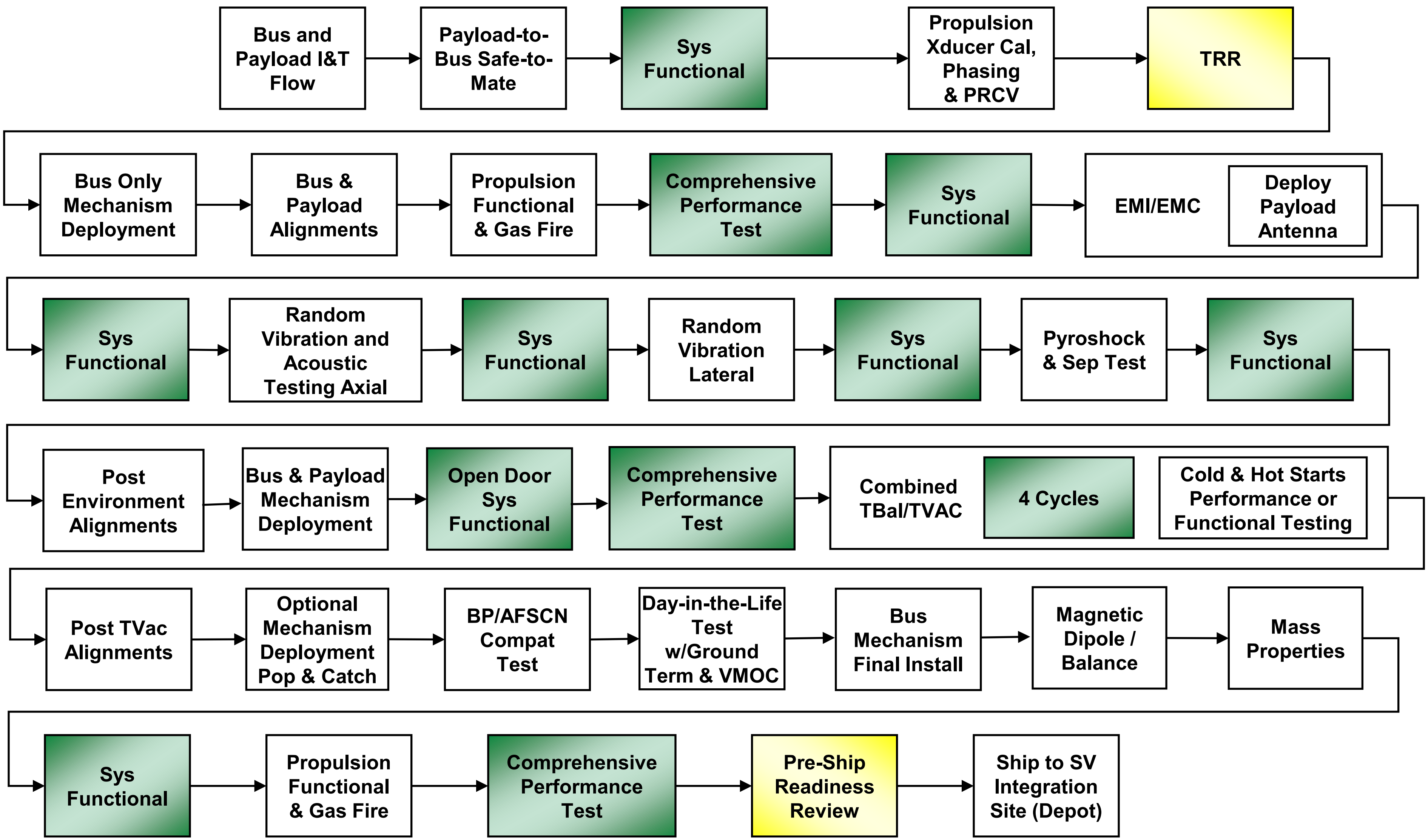
ORS BUS Generic Component Testing Flow

1. EMI Test
2. Ambient & Thermal Cycle Test
3. Stake & Coat Boards
4. Box Flight Assembly & Start of ATP
5. Ambient & Thermal Cycle Test(s)
6. 3 Axis Random Vibration
7. Ambient Test
8. Thermal Cycles *
9. Ambient Test
10. Finish Burn-In
11. Buyoff
12. Deliver for System Integration

- All Temp Cycles Are Run at Predicted Box Baseplate Temperature Extremes +/-10 Deg C
- Ambient Is 20-25 Deg C
- 9 ATP Temperature Cycles
- 2 Hour Dwells at Extremes
- Minimum of 200 Hours ATP Test Time
- Final 50 Hours Failure Free
- Static Loads Qualification by Analysis or by Sine Burst Testing

* TVAC for Battery & Transponder

Integrated SV Test Flow



Space Vehicle Testing

System Level Structural Verification

- Random Vibration Test Levels, 1 min. Duration

Frequency	PSD
20 - 250	0.004
Overall	0.96 g_{rms}

- Acceleration Response Limiting Allowed for Random Vibration
  Acceleration Responses Not to Exceed Coupled Loads Responses

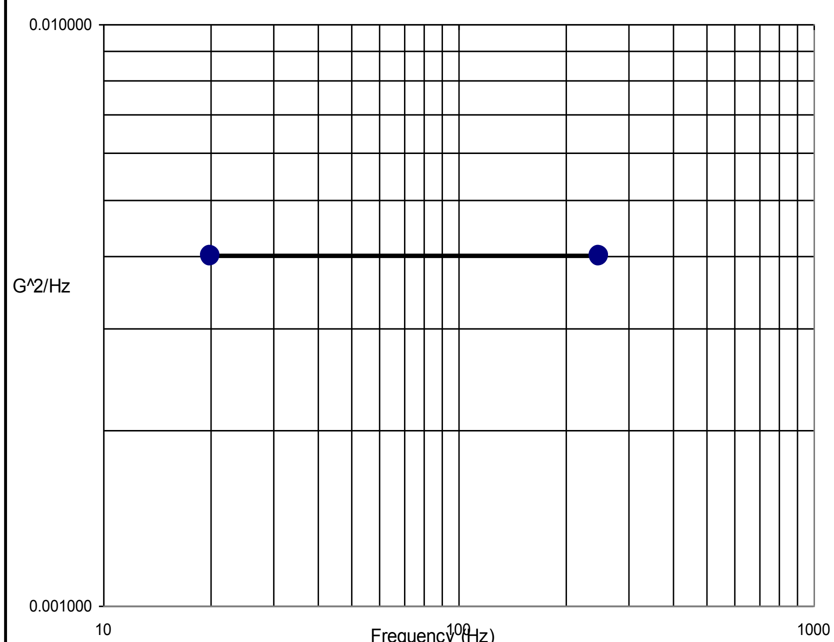
- Acoustic Test: Test Level: Overall SPL 139.2 dB
  Test Duration: One Minute

- Shock Test: Two Clamp Band Firings
  Two Solar Array Releases (Pop and Catch)

Test Levels and Durations

	Protoflight
Random Vibration	Flight + 3 dB Minimum of One Minute (Notch to Insure Responses Do Not Exceed CLA Results)
Acoustic	Flight + 3 dB Minimum of One Minute
Pyrotechnic Shock	Fire Ordnance Two Times
Thermal Vacuum	10 Degrees C Above and Below Design Range

Random Vibration Spectrum



TacSat 4 Space Vehicle Level Random Vibraton Spectrum (To be Used in Conjunction With an Acoustic Test)

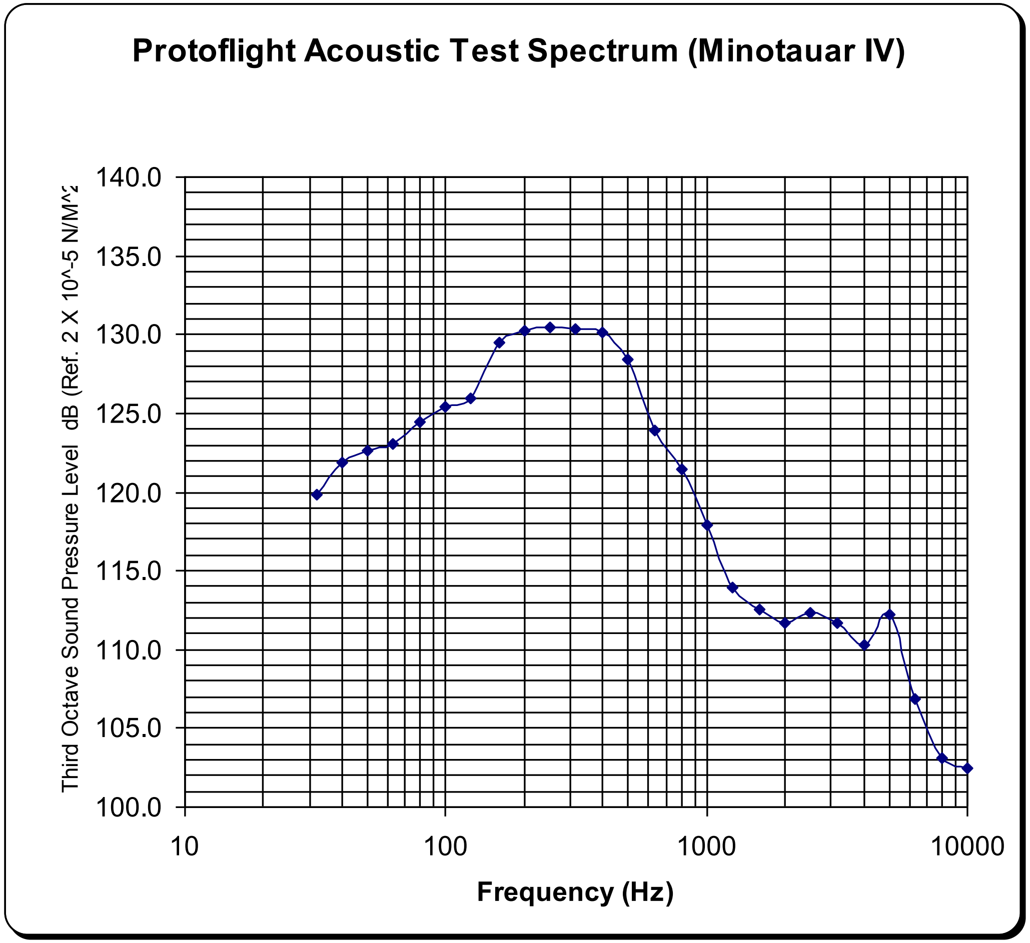
Workmanship SV Level

0.96 Grms

Frequency (Hz)	G^2/Hz
20	0.004000
250	0.004000

Apply in 3 Orthogonal Axes
One Minute per Axis

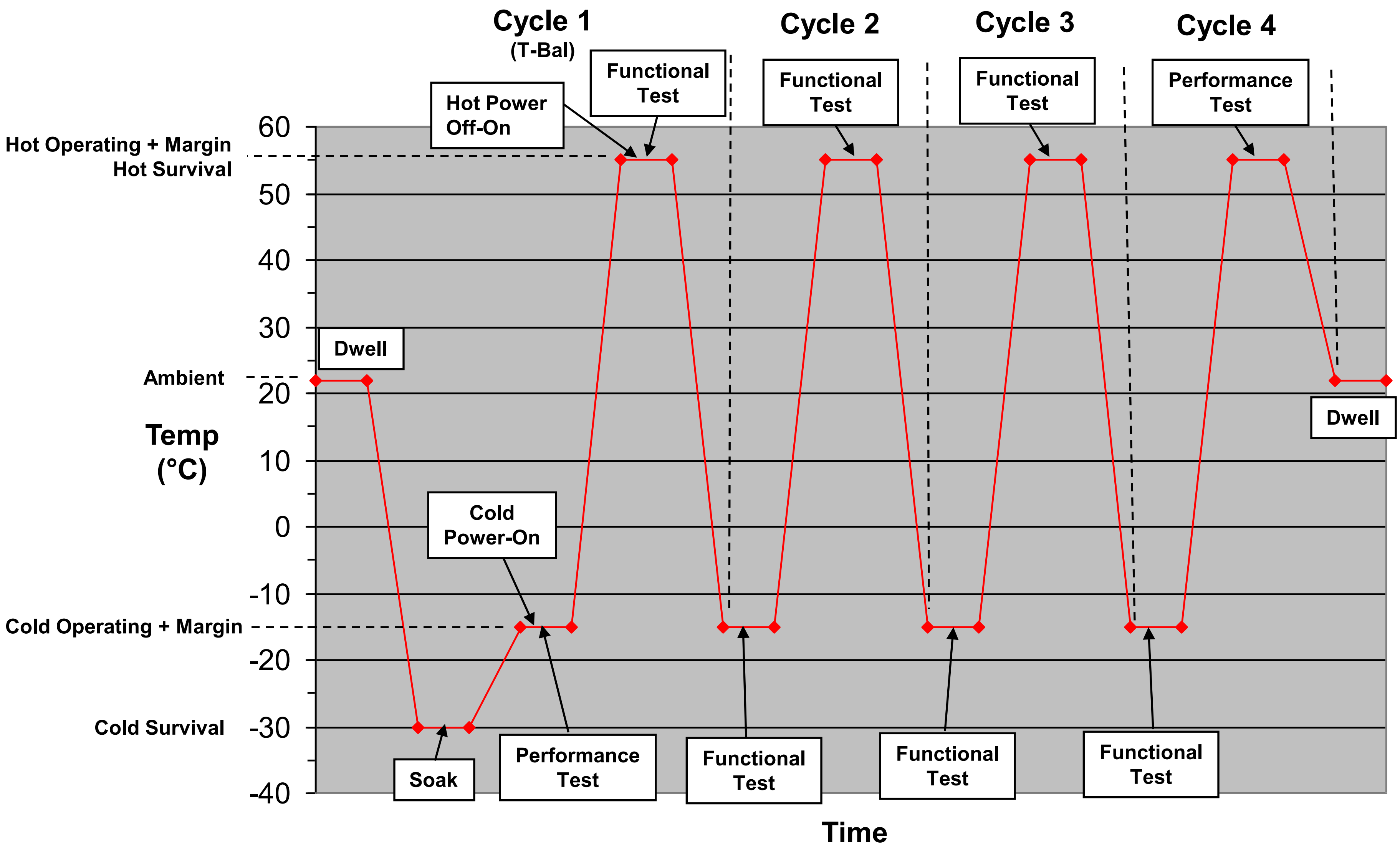
Acoustic Environment



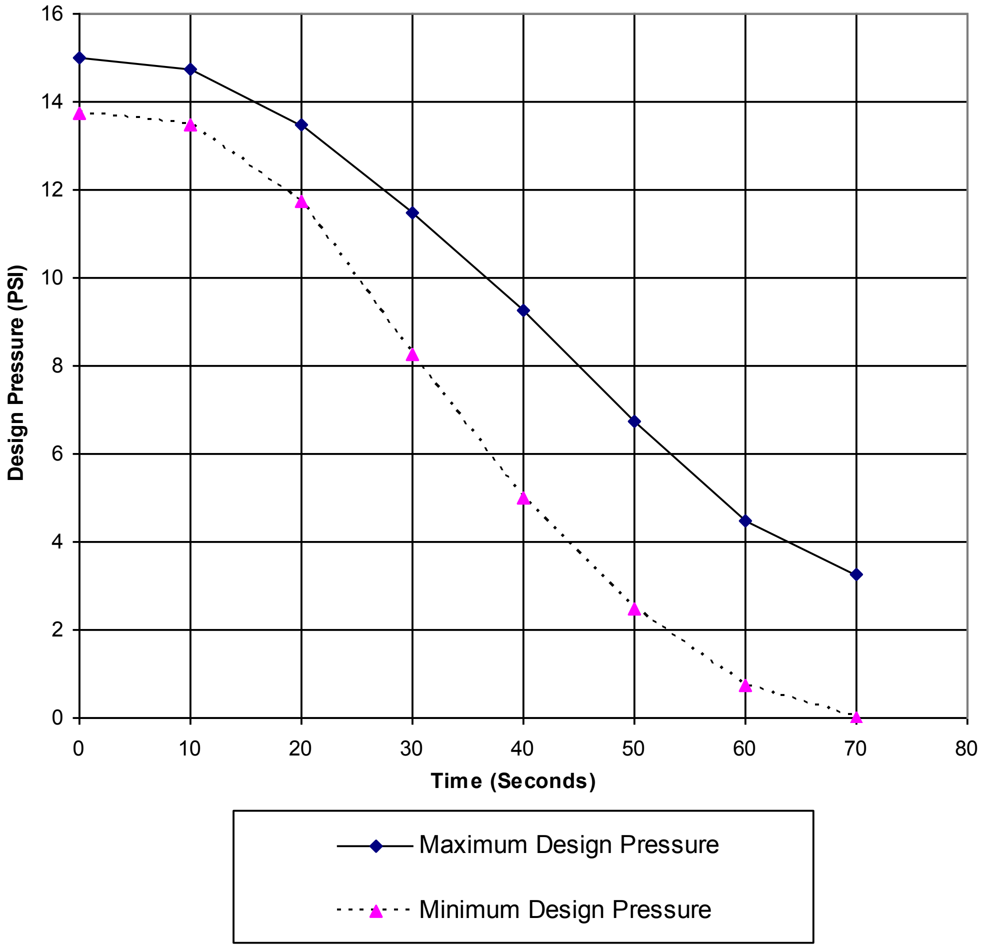
One Third Octave Frequency (Hz)	Flight Level SPL (dB)
32	119.8
40	121.9
50	122.6
63	123.1
80	124.5
100	125.4
125	125.9
160	129.5
200	130.2
250	130.5
315	130.4
400	130.1
500	128.4
630	123.9
800	121.5
1000	117.9
1250	113.9
1600	112.5
2000	111.7
2500	112.3
3150	111.7
4000	110.3
5000	112.2
6300	106.9
8000	103.1
10000	102.5
OA	139.2

Test Levels	Duration (Minutes)
Flight Unit (Protoflight Acceptance Level)	1

Thermal Balance - TVAC



Pressure Environment



Pressure History During Ascent
Maximum Decay Rate = .6 PSI / Second

Bus Integration and Test
Definition of Test Terms Continued
Mechanical Test Terminology

- *Modal Testing*
  - Characterize system's modal response relative to a reference response
- *Loads Testing/Qualification (Not shown in test flow)*
  - By Analysis With No Test Factors of Safety, or
  - Static or Quasi-Static Test at 1.25 x Design Limit Loads for the Bus
- *Vibration and Acoustic Testing*
  - Acceptance Test Levels = Expected Flight Environment for 1 Minute
  - Protoflight Test Levels = Flight +3 dB for 1 Minute
  - Qualification Test Levels = Flight +6 dB for 1 Minute
- *PyroShock and Separation Testing*
  - Twice on Flight Spacecraft
  - Light Band
- *Thermal*
  - Acceptance Test Range = 5 Deg C Above and Below Design Range
  - Protoflight Test Range = 10 Deg C Above and Below Design Range
  - Qualification Test Range = 15 Deg C Above and Below Design Range

ORS Bus Integration and Test
Definition of Test Terms Continued

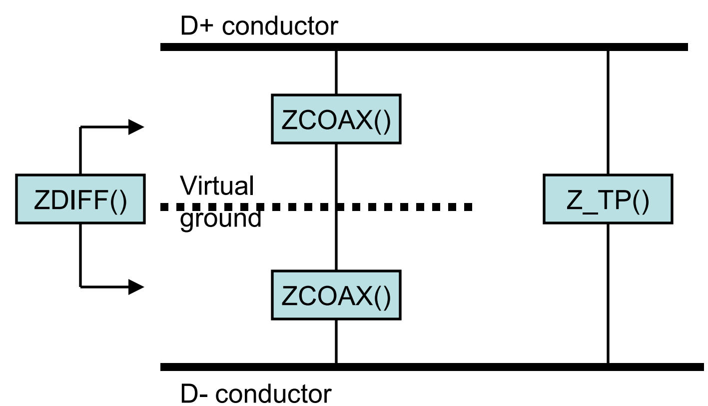
Electrical Test Terminology

- *Health Test :*
  - Test Port only, most flight like configuration
  - Typically performed at one voltage
  - Performed with the ELSE
  - Open loop testing
- *System Functional* :
  - Performed with EAGE
  - Typically performed at one voltage,
  - Partly closed loop, for ACS test cases.
  - No RF testing
- *Comprehensive Performance Test (CPT):*
  - Equivalent to System Functional
  - Performed at 3 different voltages.
  - Scripts may exercise components further than System Functional Tests
  - Includes open loop testing e.g. RF, EPS, TCS, mechanisms, and payload sim telemetry
- *Day in the life test :*
  - Performed with EAGE
  - Typically performed at predicted beginning of life voltage
  - Testing script reflects expected orbital environments
  - System is exercised and reacts as it would be on orbit for a given orbital day

Quick Formulas for Impedance Calculations

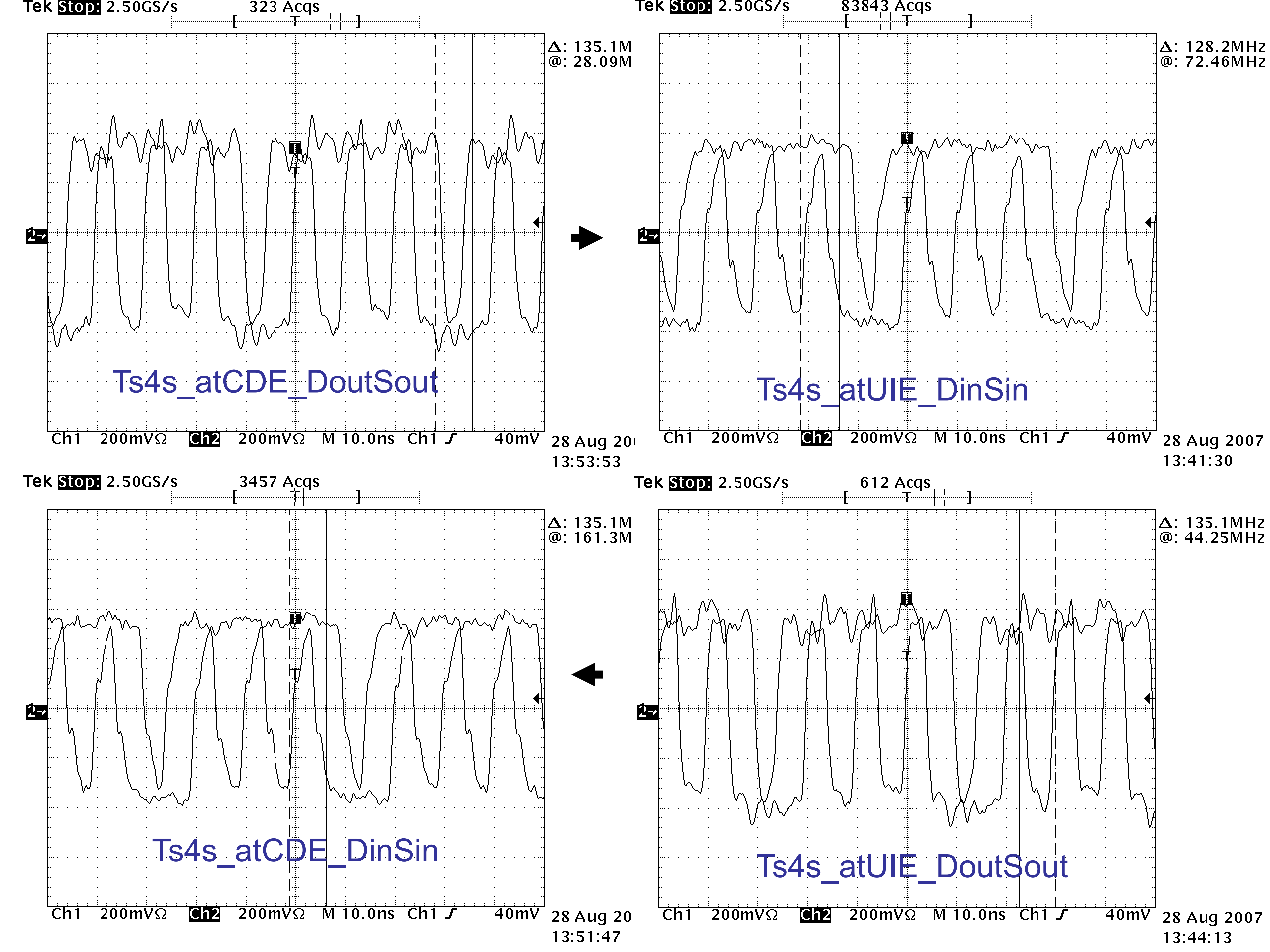
ε0 =	8.85E-12	F/m	μ0 =	1.25664E-06	H/m											
	Inner		Outer													
εr	AWG	OD	OOD	Wire Dia	Z_coax	Z_tp	Z_diff_est	Prop delay (ps/in)	Notes	r (mΩ/ft)	l_coax (μH/ft)	c_coax (pF/ft)	l_tp (μH/ft)	c_tp (pF/ft)	l_tot (μH/ft)	c_tot (pF/ft)
2.1	26	36	92	16	145	125	67	120	Tufflite TL medium wall 26GA TSP	40.8	1.1	66.5	0.2	12.2		
2.1	24	40	100	20	133	114	61	120	Tufflite TL medium wall 24GA TSP	25.7	1.0	72.8	0.2	13.6		
2.9	26	36	85	16	118	106	56	141	Kapton (150) 26GA TSP	40.8	1.0	96.2	0.2	16.9		
2.9	26	36	#####	16	16031	106	106	141	Kapton (150) 26GA TP	40.8	136.9	0.7	0.2	16.9		

- One of the lessons learned from this testing was a simple formula for calculating differential impedance
- The above spreadsheet has been surprisingly accurate in predicting differential impedance when compared to TDR results
- Formulas are from Johnson and Graham Appendix c, pg 428-429 and 424-425
- They are combined using the logic at right
  - For ZCOAX(), assume one conductor is at the center of the overall shield
  - Z_diff = (2*Z_coax) || Z_tp



Waveforms

- TacSat-4 (solder cups only)
- TacSat-4 (with pigtails at UIE uD)
- Blue ref cable
- Blue v. TacSat-4 (soldercup)
- TacSat-4 soldercup v. pigtail 1 of 2
- TacSat-4 soldercup v. pigtail 2 of 2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Δ: 135.1M
@: 28.09M
Ts4s_atCDE_DoutSout
Ch1 200mVΩ Ch2 200mVΩ M 10.0ns Ch1 ƒ 40mV
28 Aug 20
13:53:53
Tek Stop: 2.50GS/s 83843 Acqs
Δ: 128.2MHz
@: 72.46MHz
Ts4s_atUIE_DinSin
Ch1 200mVΩ Ch2 200mVΩ M 10.0ns Ch1 ƒ 40mV
28 Aug 2007
13:41:30
Tek Stop: 2.50GS/s 3457 Acqs
Δ: 135.1M
@: 161.3M
Ts4s_atCDE_DinSin
Ch1 200mVΩ Ch2 200mVΩ M 10.0ns Ch1 ƒ 40mV
28 Aug 20
13:51:47
Tek Stop: 2.50GS/s 612 Acqs
Δ: 135.1MHz
@: 44.25MHz
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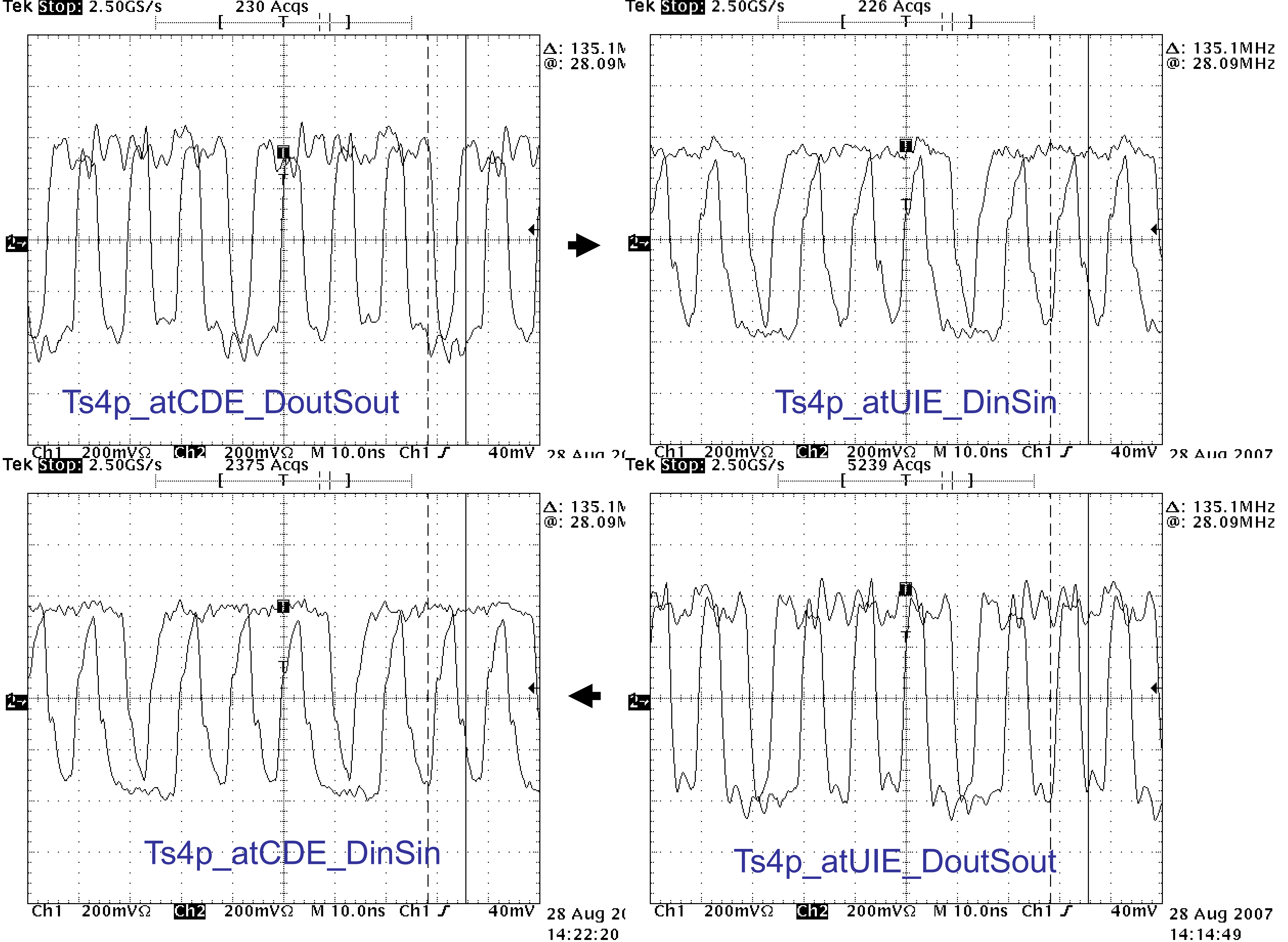
13:44:13


Tek Stop: 2.50GS/s 230 Acqs
Δ: 135.1M
@: 28.09M
Ts4p_atCDE_DoutSout
Ch1 200mVΩ Ch2 200mVΩ M 10.0ns Ch1 ƒ 40mV
Tek Stop: 2.50GS/s 226 Acqs
Δ: 135.1MHz
@: 28.09MHz
Ts4p_atUIE_DinSin
Ch1 200mVΩ Ch2 200mVΩ M 10.0ns Ch1 ƒ 40mV
Tek Stop: 2.50GS/s 2375 Acqs
Δ: 135.1M
@: 28.09M
Ts4p_atCDE_DinSin
Ch1 200mVΩ Ch2 200mVΩ M 10.0ns Ch1 ƒ 40mV
28 Aug 2(
14:22:20
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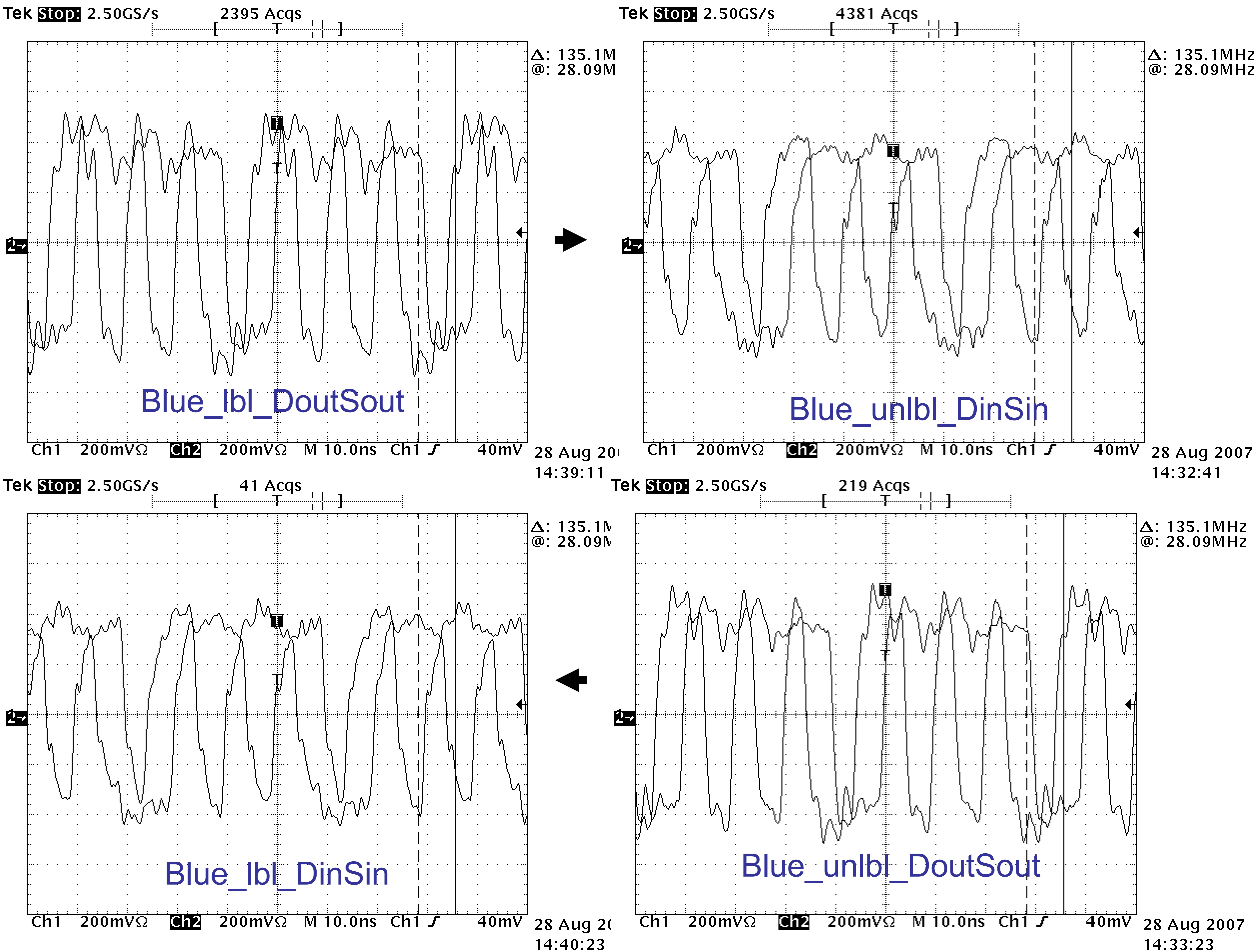

Tek Stop: 2.50GS/s 2395 Acqs
Δ: 135.1M
@: 28.09M
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28 Aug 20
14:39:11
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Δ: 135.1MHz
@: 28.09MHz
Blue_unlbl_DinSin
Ch1 200mVΩ Ch2 200mVΩ M 10.0ns Ch1 40mV
28 Aug 2007
14:32:41
Tek Stop: 2.50GS/s 41 Acqs
Δ: 135.1M
@: 28.09M
Blue_lbl_DinSin
Ch1 200mVΩ Ch2 200mVΩ M 10.0ns Ch1 40mV
28 Aug 2
14:40:23
Tek Stop: 2.50GS/s 219 Acqs
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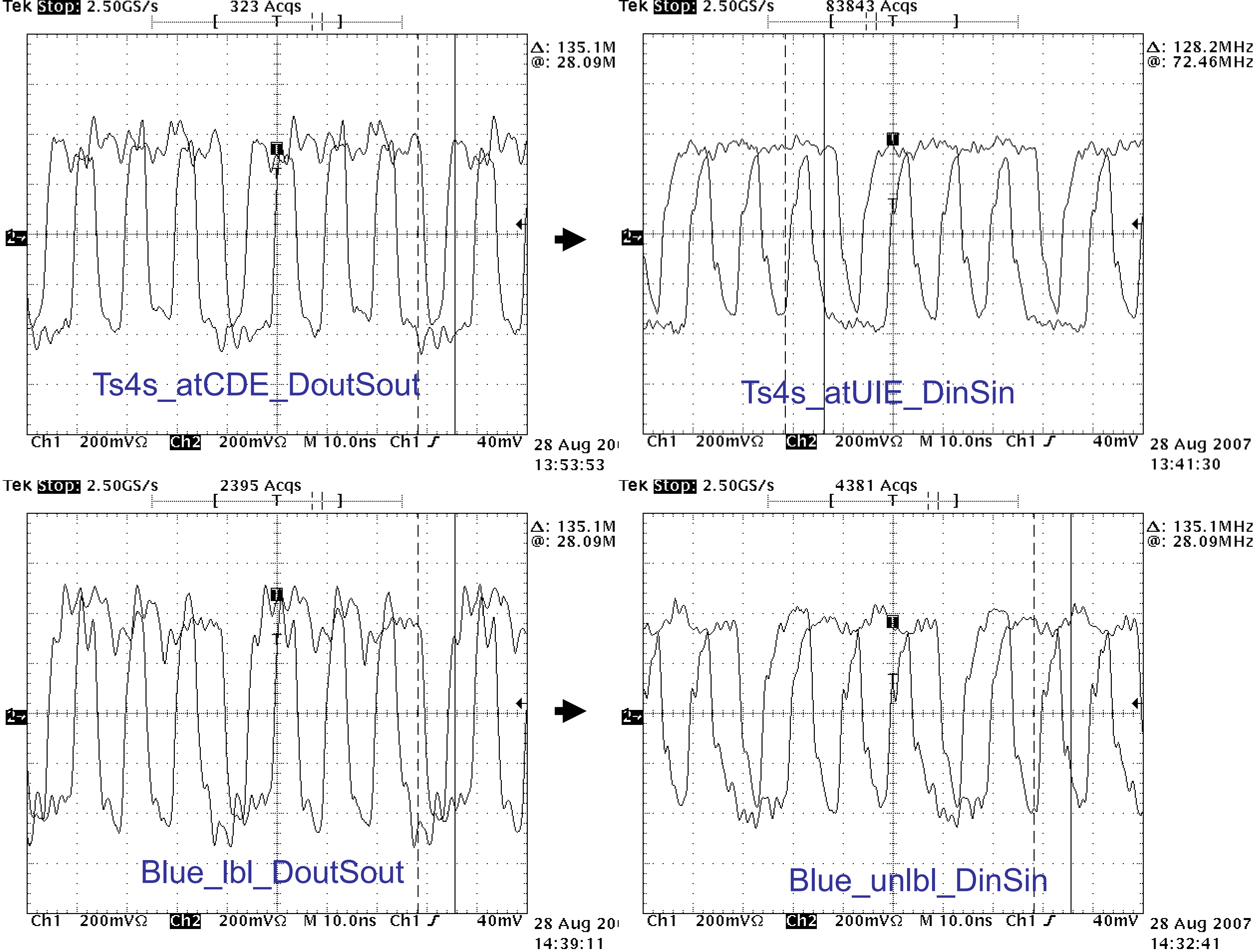
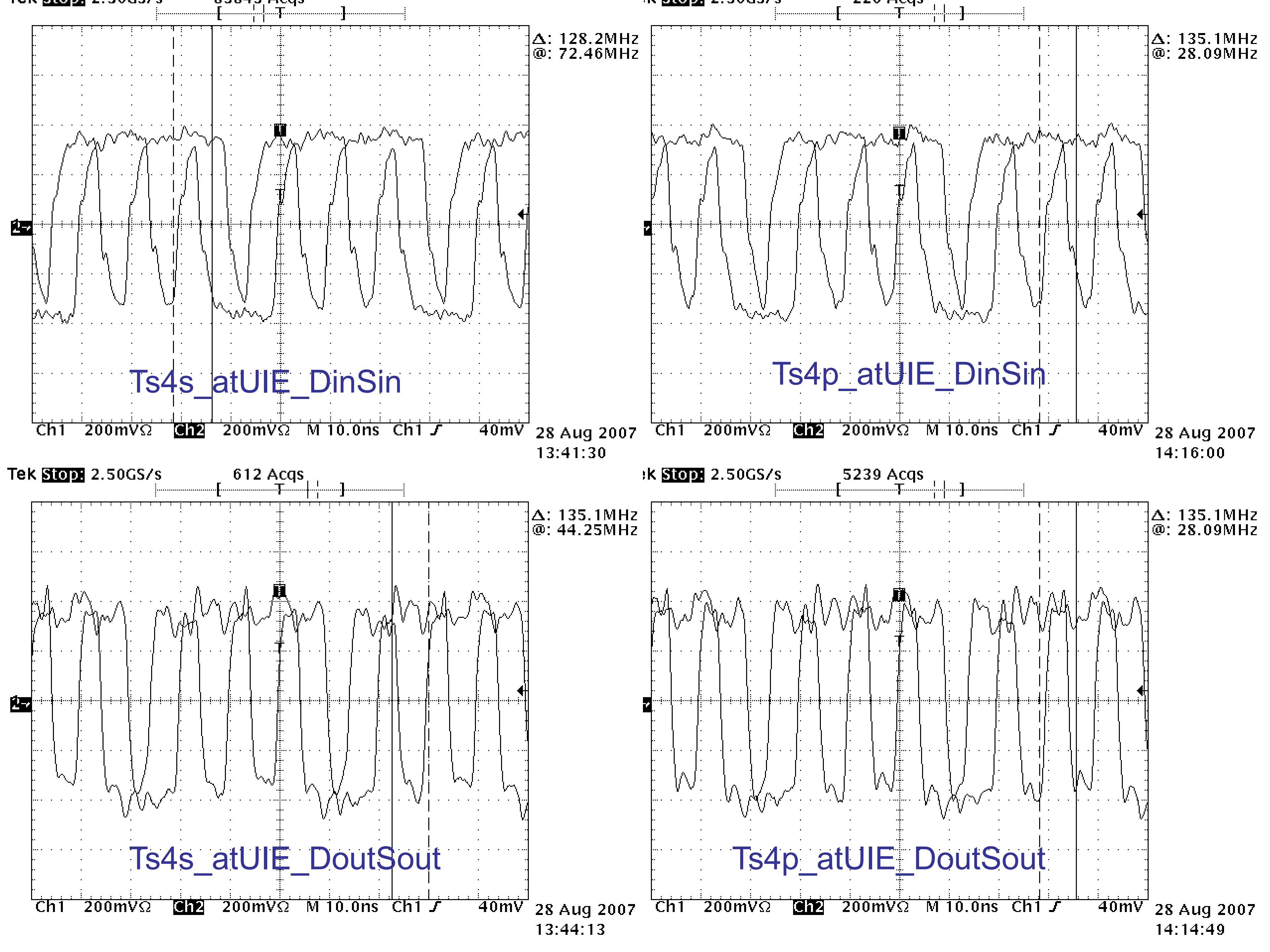
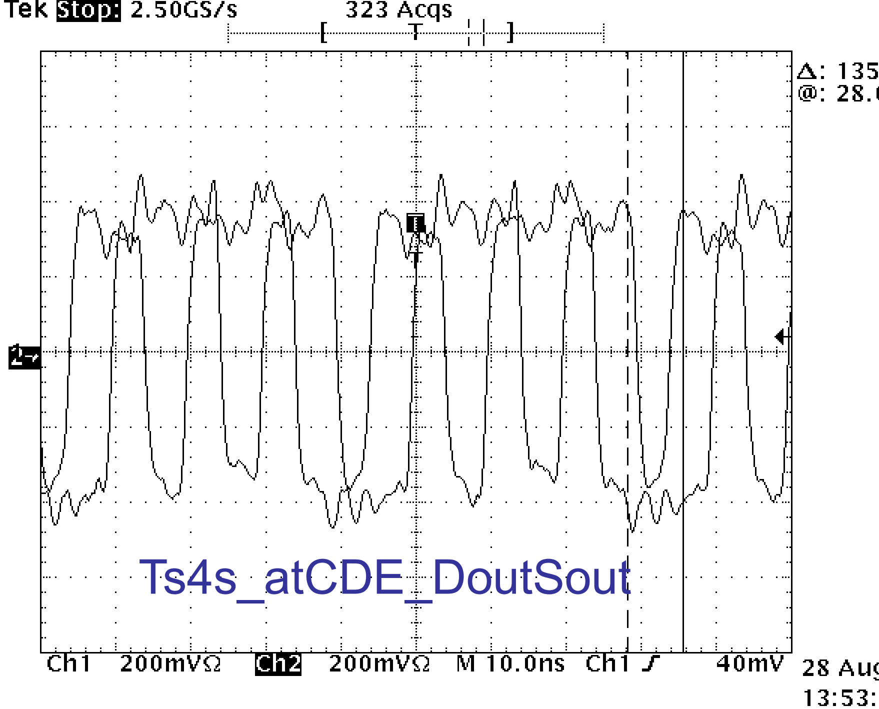
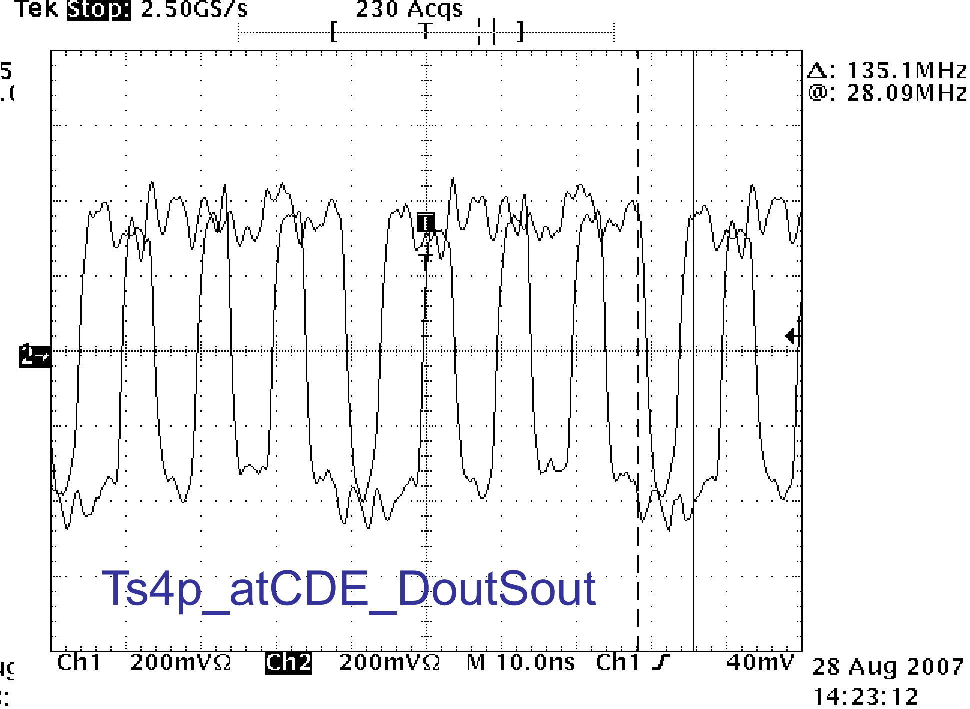
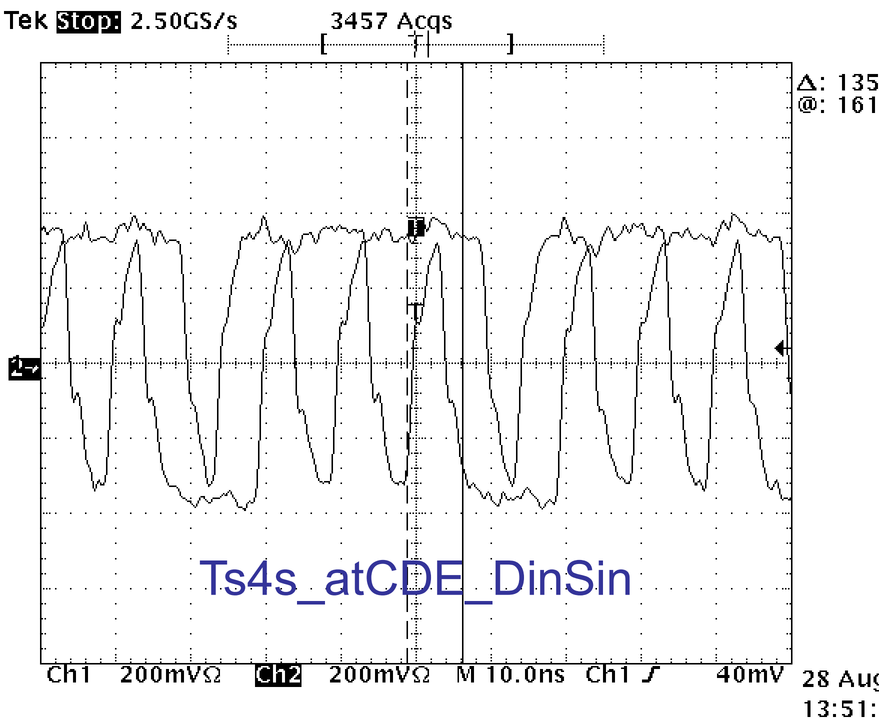
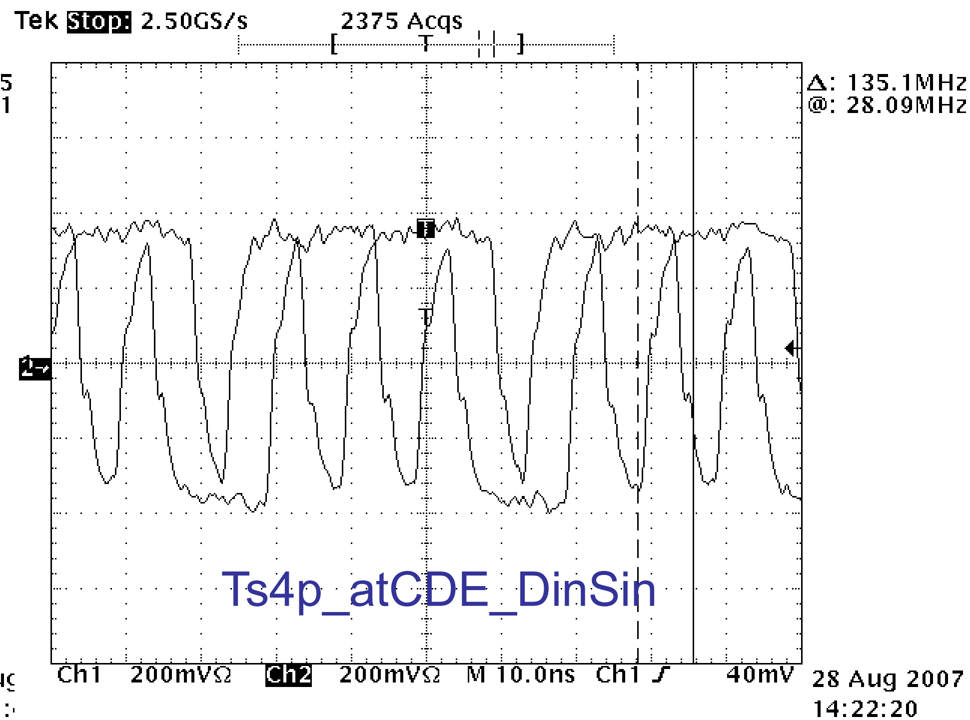

Tek Stop: 2.50GS/s 323 Acqs
Δ: 135.1M
@: 28.09M
Ts4s_atCDE_DoutSout
Ch1 200mVΩ Ch2 200mVΩ M 10.0ns Ch1 ∫ 40mV
28 Aug 20
13:53:53
Tek Stop: 2.50GS/s 83843 Acqs
Δ: 128.2MHz
@: 72.46MHz
Ts4s_atUIE_DinSin
Ch1 200mVΩ Ch2 200mVΩ M 10.0ns Ch1 ∫ 40mV
28 Aug 2007
13:41:30
Tek Stop: 2.50GS/s 2395 Acqs
Δ: 135.1M
@: 28.09M
Blue_lbl_DoutSout
Ch1 200mVΩ Ch2 200mVΩ M 10.0ns Ch1 ∫ 40mV
28 Aug 20
14:39:11
Tek Stop: 2.50GS/s 4381 Acqs
Δ: 135.1MHz
@: 28.09MHz
Blue_unlbl_DinSin
Ch1 200mVΩ Ch2 200mVΩ M 10.0ns Ch1 ∫ 40mV
28 Aug 2007
14:32:41


Δ: 128.2MHz
@: 72.46MHz
Ts4s_atUIE_DinSin
Ch1 200mVΩ Ch2 200mVΩ M 10.0ns Ch1 40mV
28 Aug 2007
13:41:30
Δ: 135.1MHz
@: 28.09MHz
Ts4p_atUIE_DinSin
Ch1 200mVΩ Ch2 200mVΩ M 10.0ns Ch1 40mV
28 Aug 2007
14:16:00
Tek Stop: 2.50GS/s
612 Acqs
Δ: 135.1MHz
@: 44.25MHz
Ts4s_atUIE_DoutSout
Ch1 200mVΩ Ch2 200mVΩ M 10.0ns Ch1 40mV
28 Aug 2007
13:44:13
Stop: 2.50GS/s
5239 Acqs
Δ: 135.1MHz
@: 28.09MHz
Ts4p_atUIE_DoutSout
Ch1 200mVΩ Ch2 200mVΩ M 10.0ns Ch1 40mV
28 Aug 2007
14:14:49


Tek Stop: 2.50GS/s
323 Acqs
Δ: 135
@: 28.(
Ts4s_atCDE_DoutSout
Ch1 200mVΩ Ch2 200mVΩ M 10.0ns Ch1 ƒ 40mV
28 Aug
13:53:


Tek Stop: 2.50GS/s
230 Acqs
Δ: 135.1MHz
@: 28.09MHz
Ts4p_atCDE_DoutSout
Ch1 200mVΩ Ch2 200mVΩ M 10.0ns Ch1 ƒ 40mV
28 Aug 2007
14:23:12


Tek Stop: 2.50GS/s
3457 Acqs
Δ: 135
@: 161
Ts4s_atCDE_DinSin
Ch1 200mVΩ Ch2 200mVΩ M 10.0ns Ch1 ƒ 40mV
28 Aug
13:51:


Tek Stop: 2.50GS/s
2375 Acqs
Δ: 135.1MHz
@: 28.09MHz
Ts4p_atCDE_DinSin
Ch1 200mVΩ Ch2 200mVΩ M 10.0ns Ch1 ƒ 40mV
28 Aug 2007
14:22:20

Distances, times to remember

- Segments lengths in inches, 1 way transit time, and round trip transit time
  - TS4 cables, er = ~1.5, prop velocity = 250ps/in
    - CDE to Bus IF = 36”, 6.5ns(1w)/13ns(rt)
    - Bus IF to Payload IF = 48 ”, 12ns(1w)/24ns(rt)
    - Payload IF to UIE = 50 ”, 12.5ns(1w)/25ns(rt)
    - CDE to Payload IF = 84”, 21ns(1w)/42ns(rt)
    - UIE to Bus IF = 98”, 24.5ns(1w)/49ns(rt)
    - Total length = 134”, 33.5ns(1w)/67ns(rt)
  - Blue Ref cable, er = ~3 (guess), prop velocity = 170ps/in
    - Total length = 26”, 4.4ns(1w)/8.8ns(rt)

Recent NRL High Speed Data Designs

- NPOESS Firewire, Ken Wolfram
  - Link, DPHY, and APHY chips
- STEREO (SECCHI)
  - Board Design by Greg Clifford, of SEI.
  - Details available from Greg Clifford (gclifford@silvereng.com) or via SECCHI design review material
  - Of note:
    - SECCHI TVAC cables were created and used with 37P circular connector inline
      - 3 pairs of COTS spacewire (DVI heritage) cables were cut up and a 37P circular connector (D507-37S-059) was attached to the end.
      - A DM5623-37PP was used to penetrate the chamber wall
      - The vacuum portion of the cable assembly was created with 26GA TSP and an overall shield. This terminated in uDs on the UUT end and a 37S Circular on the chamber wall end (13084 37S-5020)
    - No additional qualification, no signal integrity testing was done on the cable solution
    - Cable configuration worked fine at 100Mb/s
    - Only problems encountered were workmanship:
      - The 28GA wire in the COTS cables kept coming loose from the 37-CIR
    - Flight cables were COTS spacewire

Derek Schierlmann Background

- Electronics Engineer, NRL 2003- present
  - Electrical I&T lead TACSAT-4 / ORS phase-3 bus
- Hardware Design Engineer, Hewlett-Packard Technical Workstation Laboratory 2000-2003
  - USB Subsystem Lead Engineer
- Senior Software Support Engineer, Hewlett-Packard 1995 - 2000
- Masters of Electrical Engineering, Colorado State University, 2003
- Master's thesis: *Transmission time prediction for meander delay lines in a common PCB geometry*
  - Use of Ansoft HFSS, HPSpice and Matlab to suggest an equation to quantify the actual propagation speed of a signal through a meandering delay line of printed circuit board traces.
- Bachelors of Electrical Engineering, Auburn University 1993