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A System-On-Chip Radiation Hardened Microcontroller ASIC With Embedded SpaceWire Router

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Introduction / Project Goals

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- The RAD6000MC™ microcontroller is being designed to consolidate all the key elements needed for moderate levels of spaceborne computing into a single ASIC
- It is flexible enough for a wide variety of applications, from instrument control to “safe mode” back-up
- The RAD6000MC will be manufactured in BAE Systems’ RH15 150nm radiation hardened technology, with a goal of 10x improvement in power-performance vs. existing RAD600-based single board computers
- Based on the space-proven RAD6000 CPU, it will include strong software support for users
  - **Green Hills Compiler**
  - **VxWorks operating system** with possible addition of real time embedded solution as well
  - Easy reuse/migration of existing RAD6000 application code
  - Reuse of existing RAD6000 infrastructure

RAD6000MC™ Features

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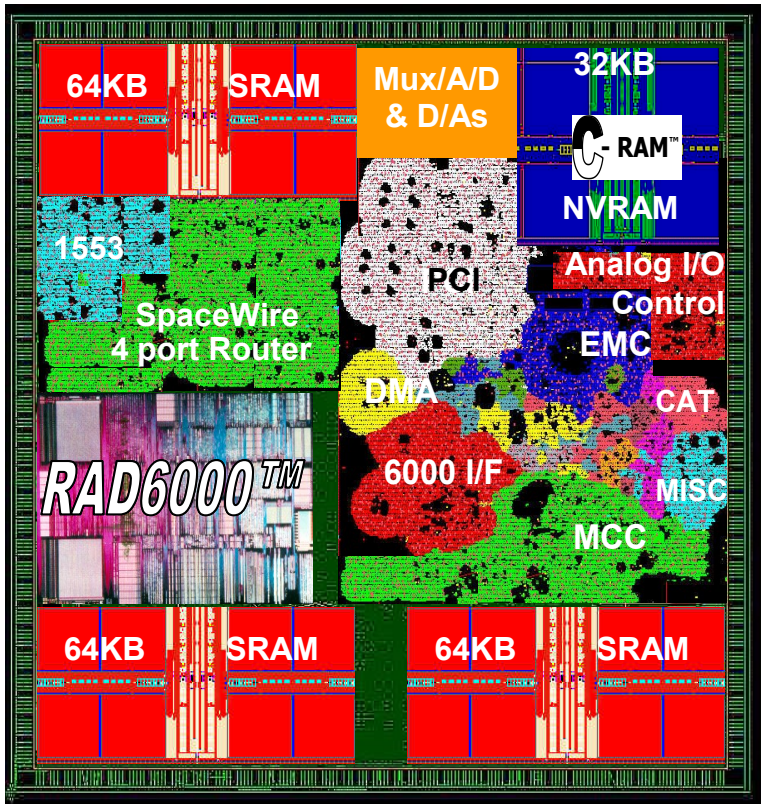

- **Planned Radiation Characteristics**
  - Total Dose: ***1Mrad (Si)***
  - Single Event Effects
    - ***<1E-10 errors/bit-day***
    - Latch-up immune

- **Processor Units**
  - **RAD6000™ CPU**
    - Selectable 33 or 66 MHz clock
    - Fixed and floating point execution units
    - Up to 3 instructions/cycle
    - 8KB unified D/I cache
  - Embedded Microcontroller (EMC)
- **SRAM and Non-volatile Memory with controllers**
  - **128 KB synchronous SRAM** on-chip memory
  - **32 KB C-RAM™** non-volatile program store
  - External Memory controller for SRAM, DRAM, C-RAM, etc.
  - Direct Memory Access (DMA) controller
- **I/O Bus and Communications Interfaces**
  - 33 MHz, **64-bit PCI** interface (version 2.2)
  - 16550 compatible **UART**
  - **SpaceWire router** with **4 serial links**
  - Dual **1553** interface **w/64 KB of on-chip SRAM**
- **JTAG master and slave test controllers**
- **Analog interfaces**
  - 12-bit, 8.25 Msps **A-D converter**
  - 48 input programmable analog multiplexer
  - Three 12-bit 1 Ksps **D-A converters**

Conceptual layout shown

RAD6000MC ASIC Block Diagram

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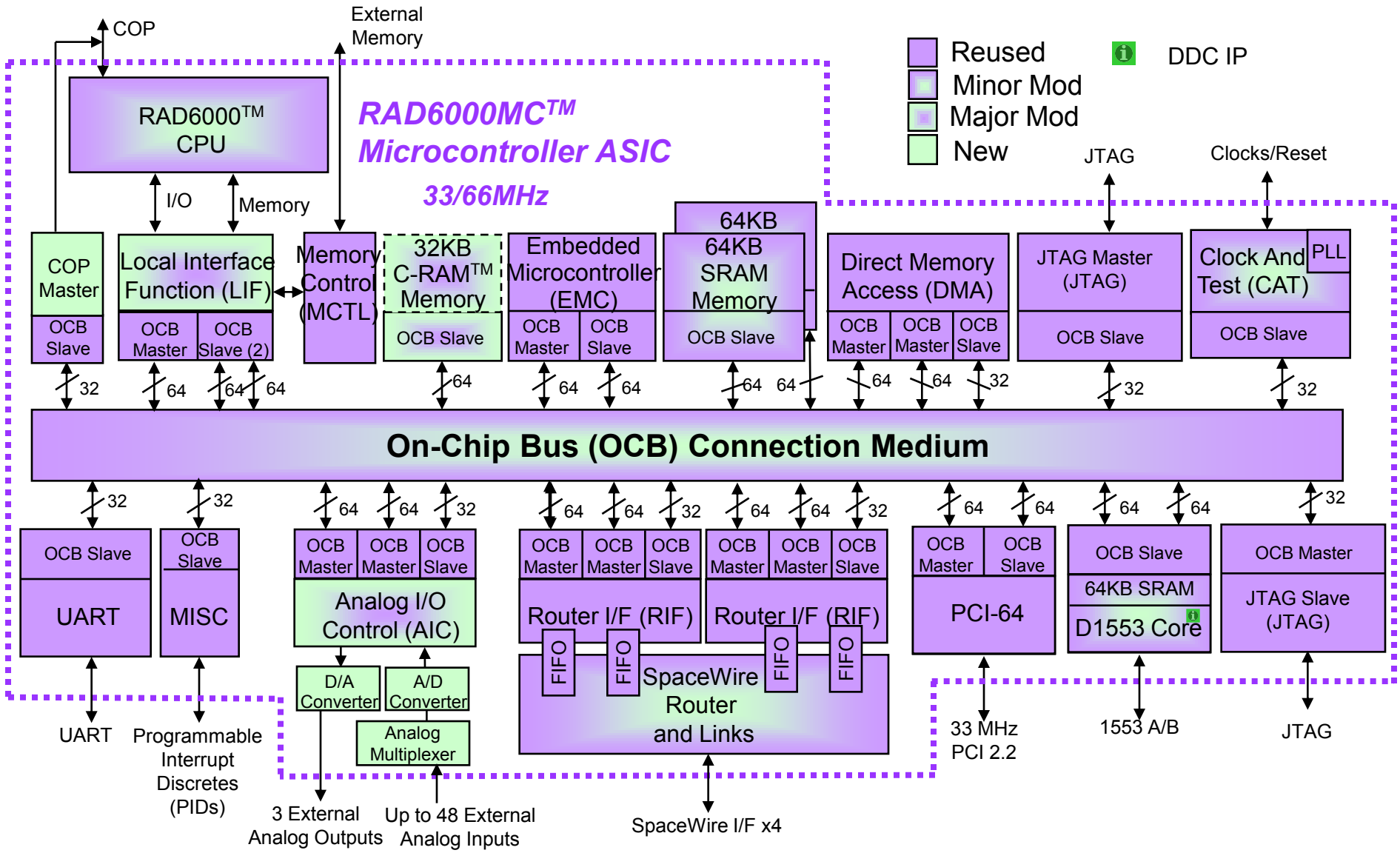

RAD6000 Microprocessor

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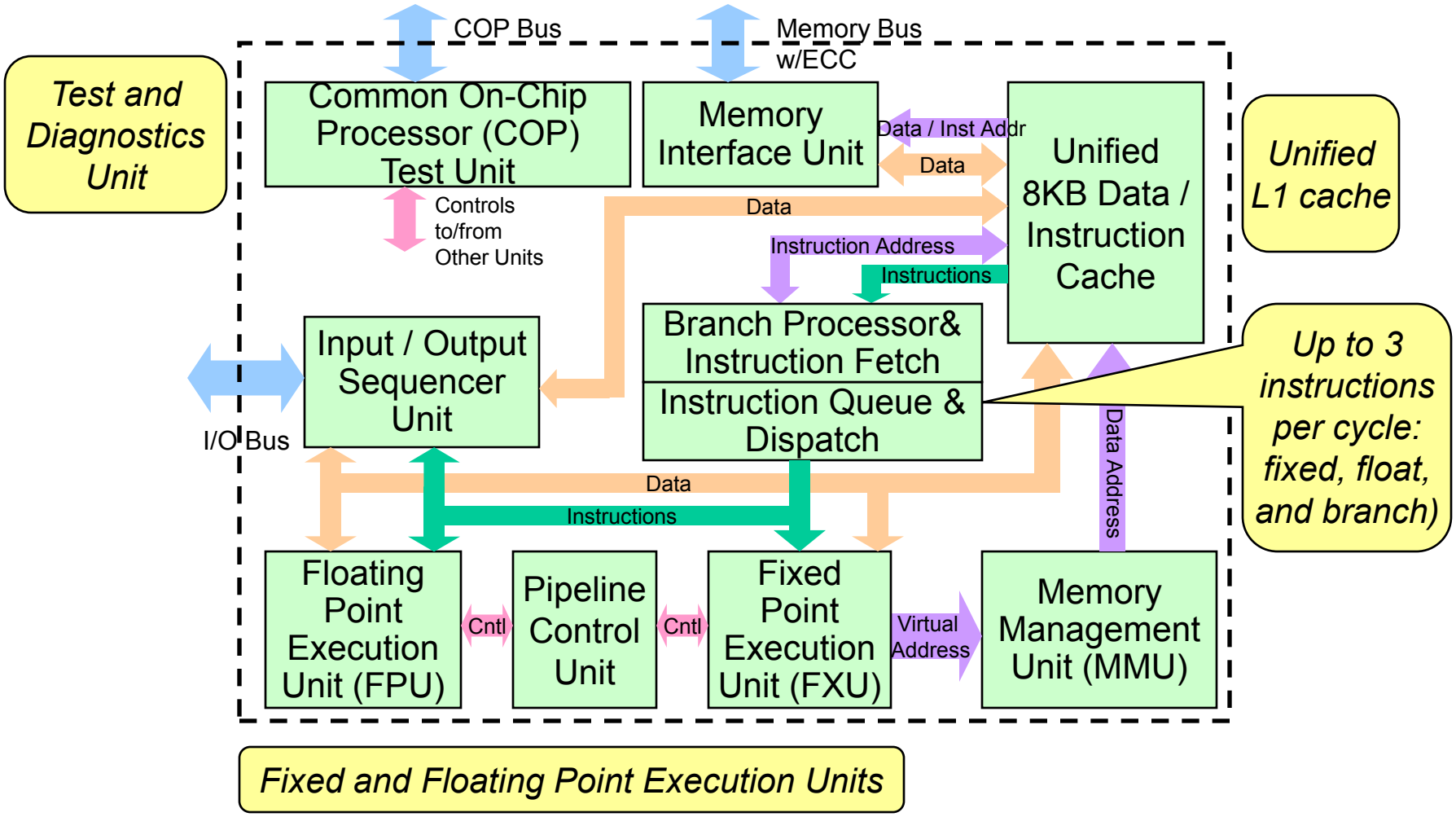

Local Interface Function (LIF) Block Diagram

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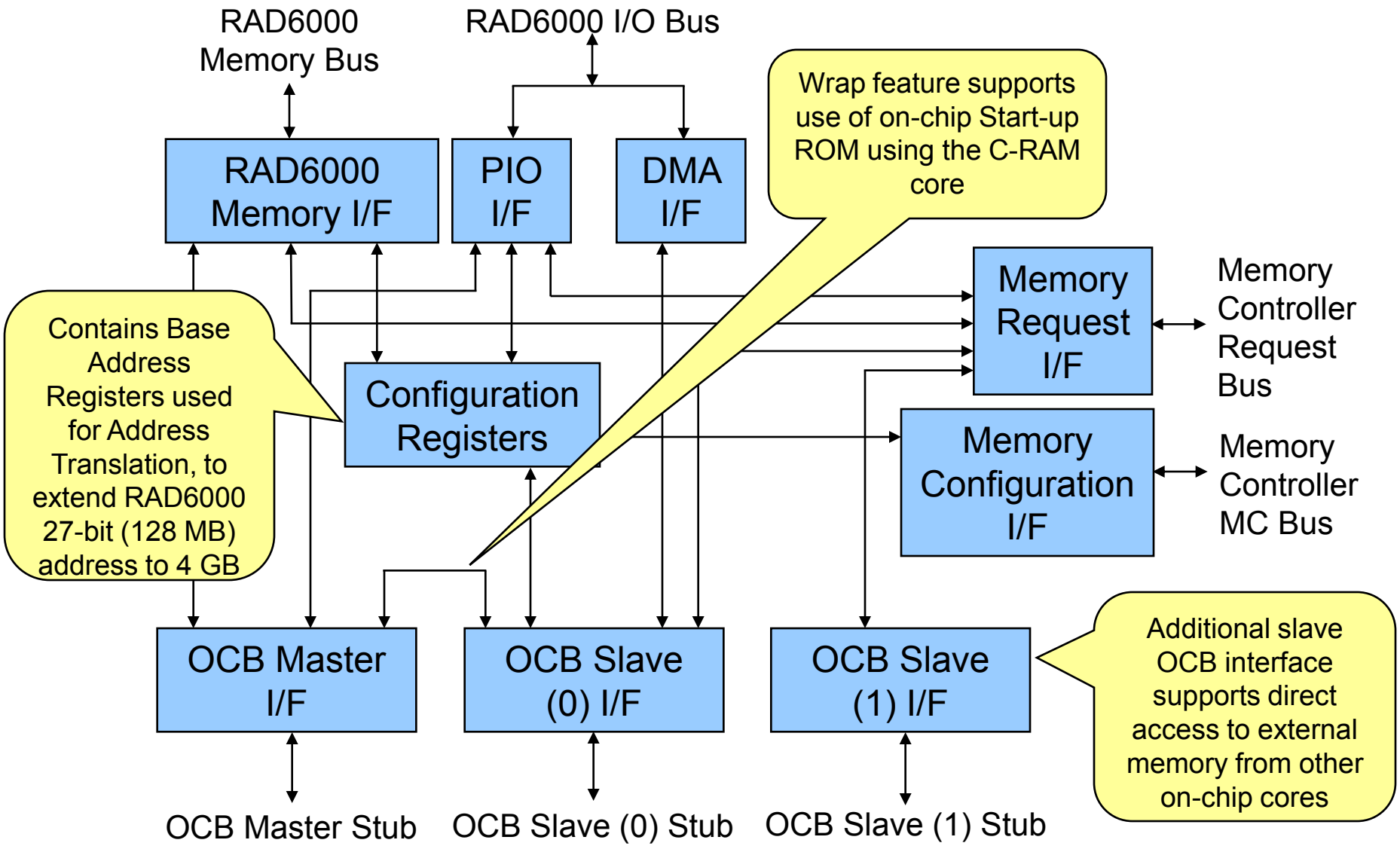

RAD6000 Memory Address Translation

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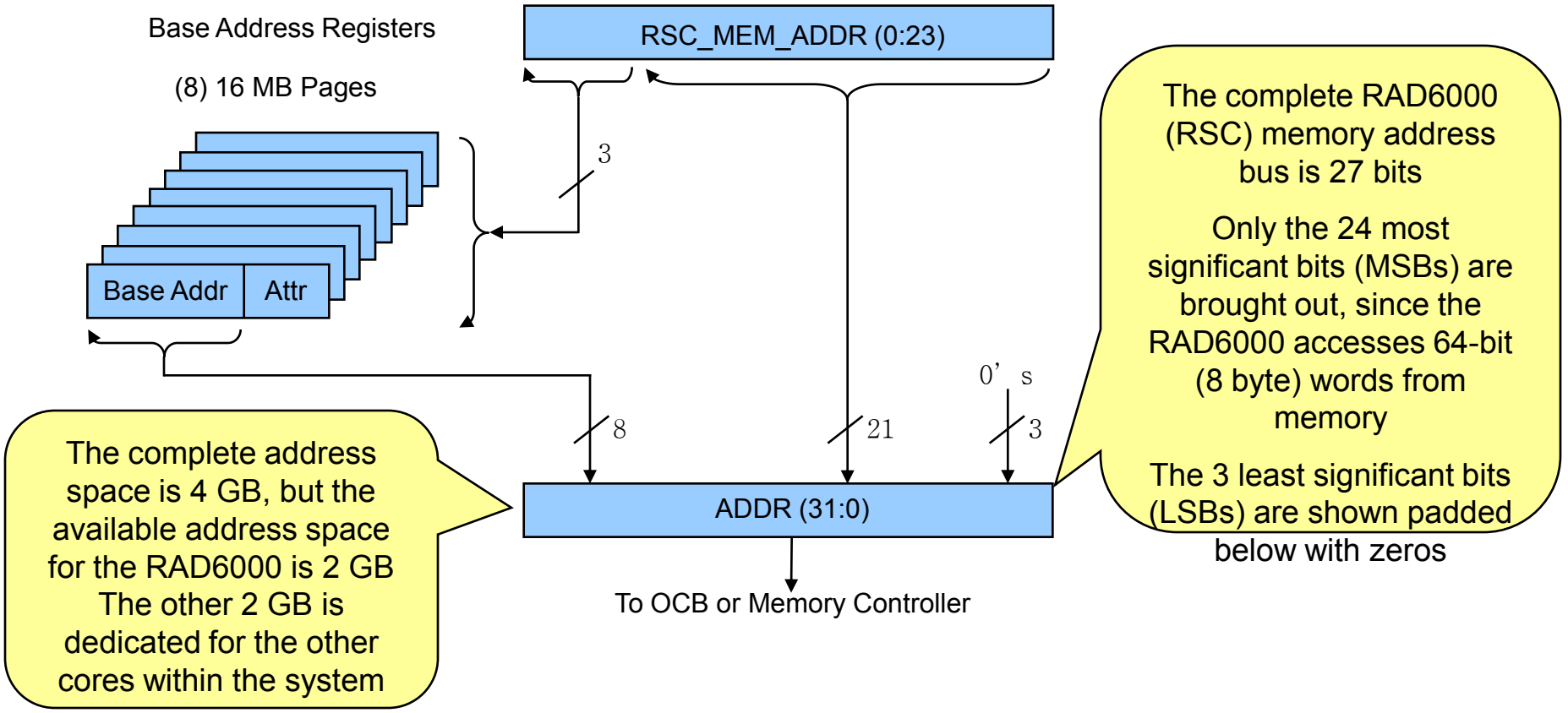

On-Chip Bus Slave Memory Address Translation

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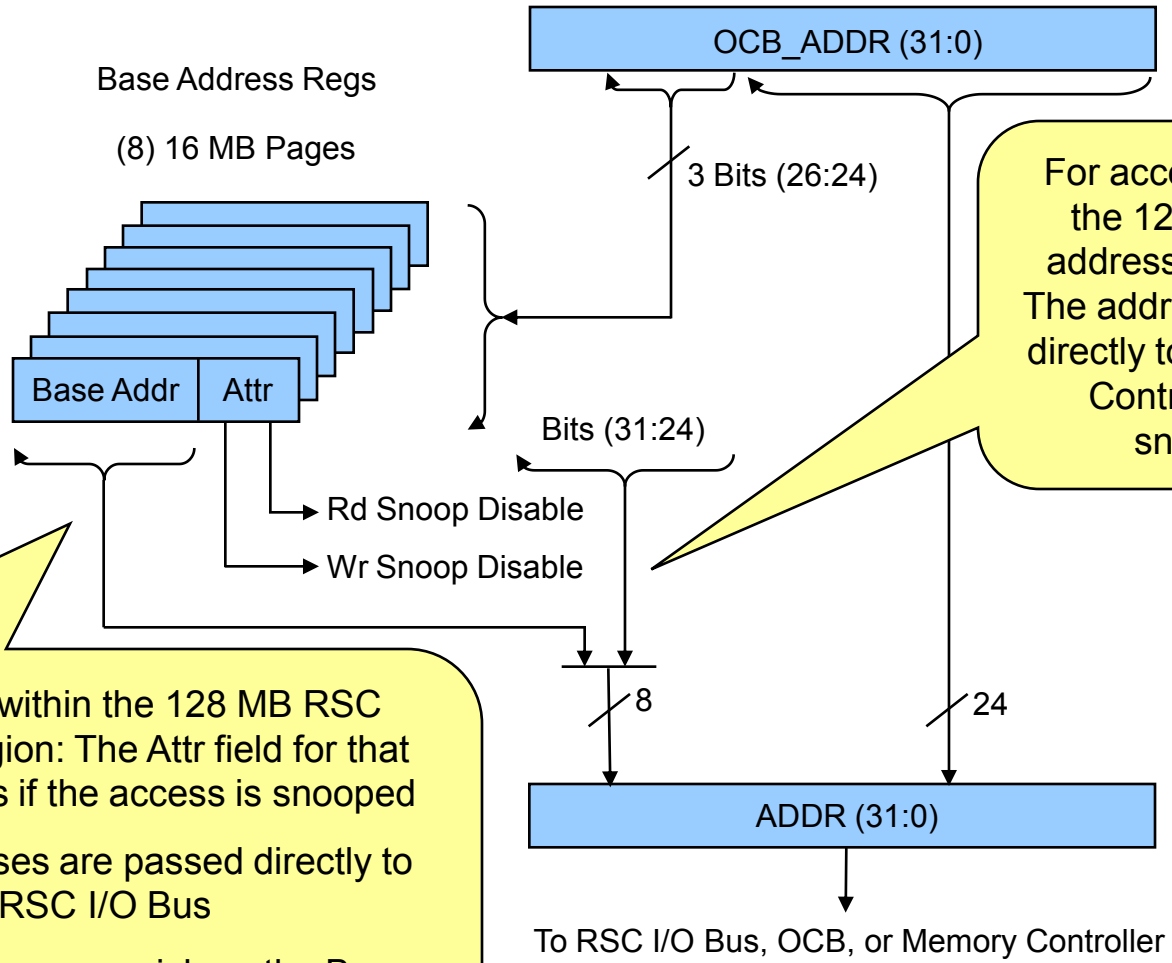

For accesses above the 128 MB RSC addressable region: The address is passed directly to the Memory Controller – no snooping

For accesses within the 128 MB RSC addressable region: The Attr field for that page determines if the access is snooped

Snooped accesses are passed directly to the RSC I/O Bus

Non-snooped accesses pick up the Base Addr field for the page and then are passed to either the Memory Controller or OCB

SpaceWire Router Block Diagram and Features

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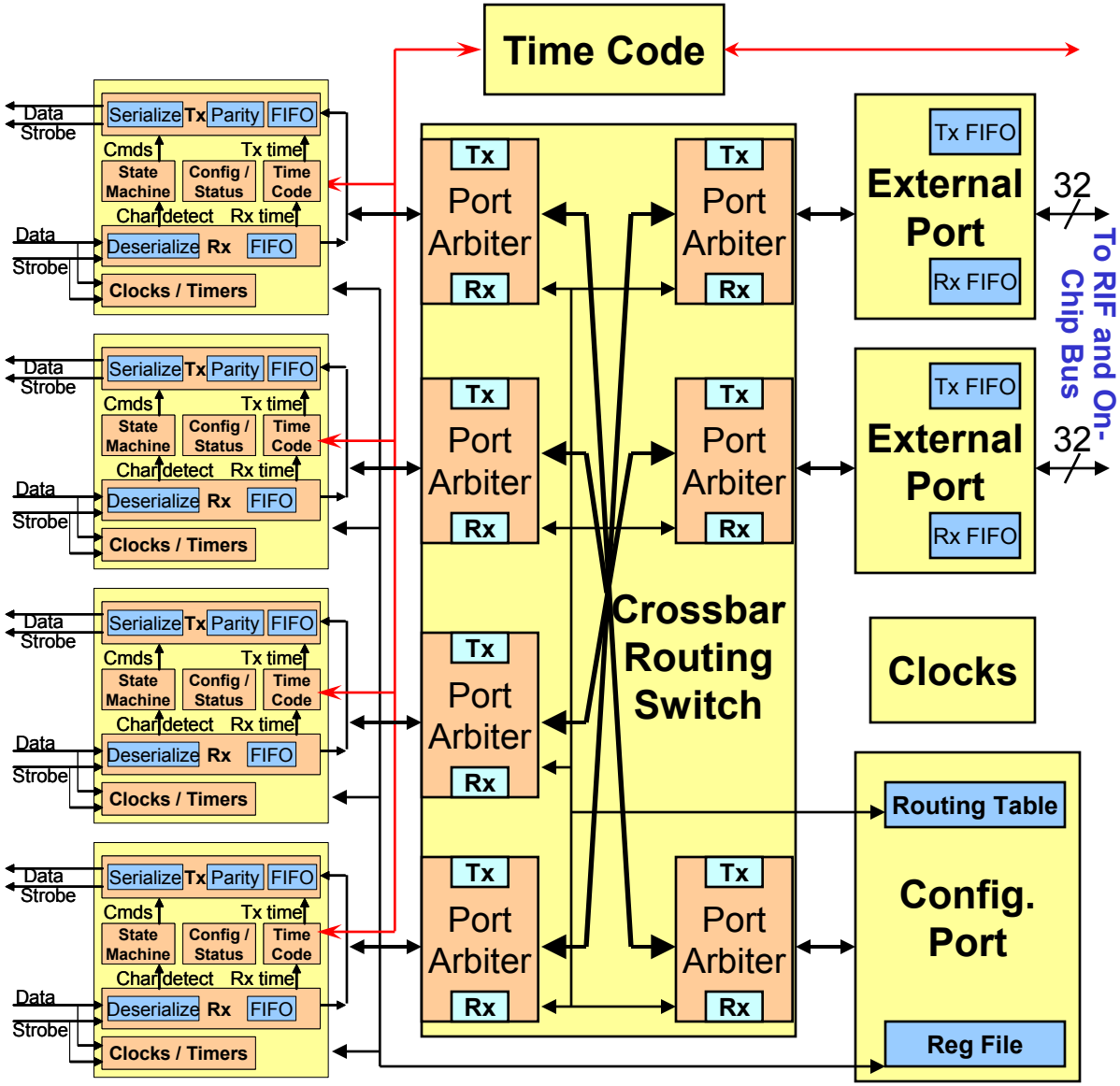

- SpaceWire core implementation
  - Four SpaceWire ports include integrated LVDS drivers / receivers with support for cold sparing
  - Dual ports connected to On-Chip Bus increase throughput
  - 350 MHz maximum data rate on SpaceWire link interfaces
- Unique switch enhancements
  - Bypass Mode ignores SpaceWire addressing and fixes route assignment for packet
  - Local header byte indicates port # received from and presence of Logical Address
  - Network blockage mitigation by limiting packet length limits risk of network stalling

Programmable Multiplexer and A/D Converter

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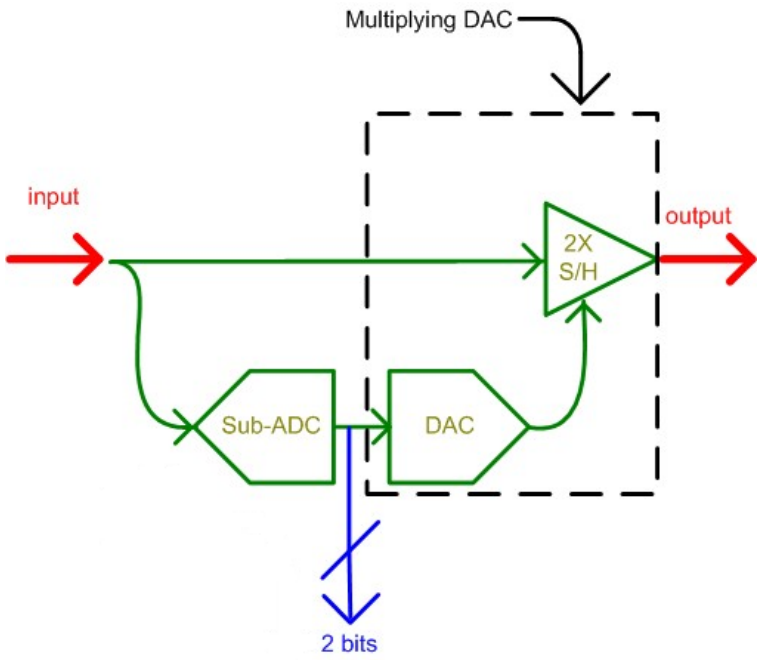
All (48) Single Ended Inputs	32 Single Ended	16 Single Ended	All (24) Differential Inputs
	And 8 Differential	and 16 Differential	

- Analog Multiplexer with programmable input configurations, supporting single-ended, differential, or mixed input signals
- Select signals controlled from Analog I/O Control digital core



- 12-bit Pipeline A/D converter with 1.5 bits per stage (single stage shown)
- High performance Sample and Hold circuit with Operational Transconductance Amplifiers
- Digital error correction tolerates 500 mV of comparator offset
- Supported by Bandgap Reference circuit to generate differential reference voltage

Wilkinson Architecture Three Channel D/A Converter

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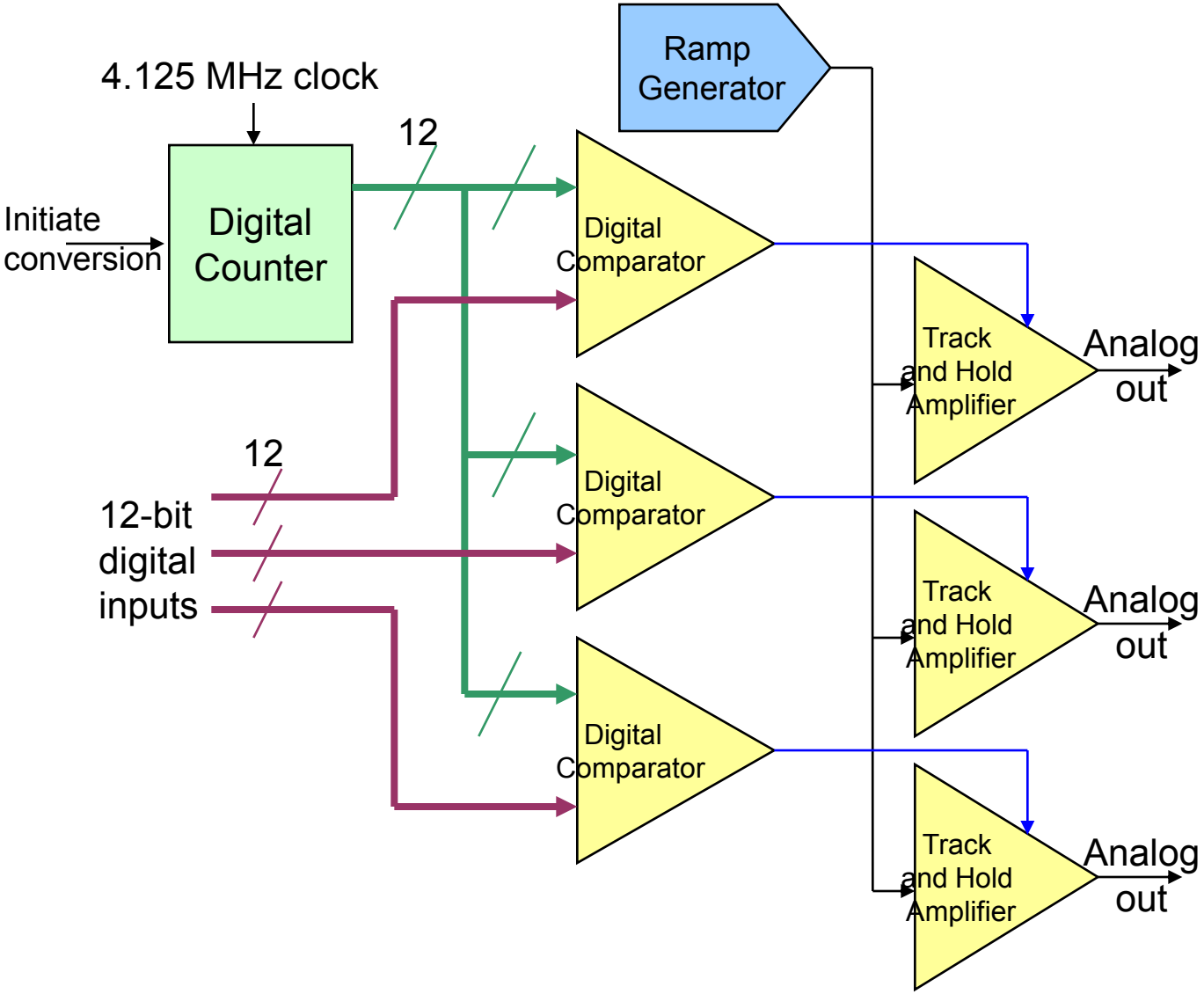

- Wilkinson D/A converter architecture
  - Shared ramp generator and digital counter
  - Repeated comparators and track and hold amps
- Pipelined gray code digital counter uses 4,096 cycles for 12 bit resolution @ 1 Ksps
- Track and Hold samples ramp voltage when comparator pulses
- Minimal die and power dissipation for low speed conversion

Analog Circuit Test Chips

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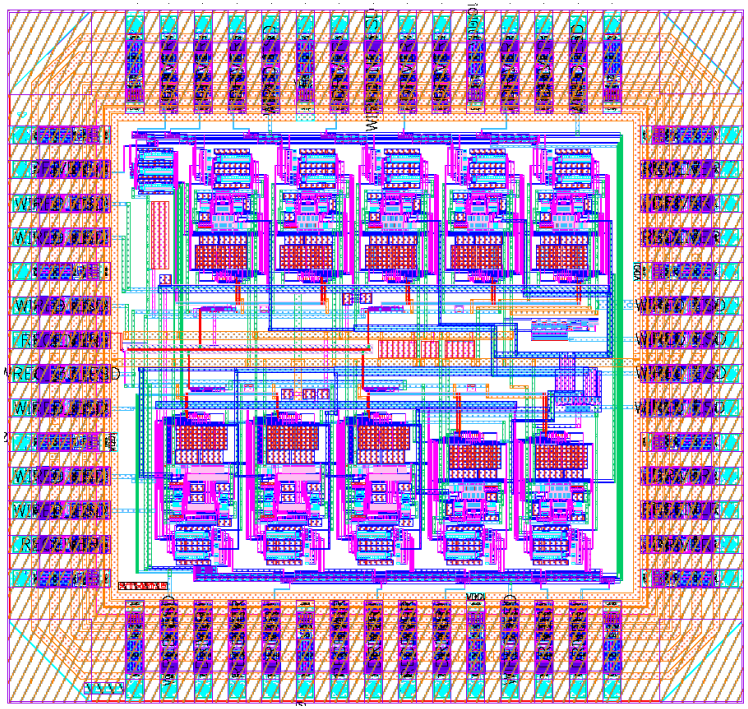
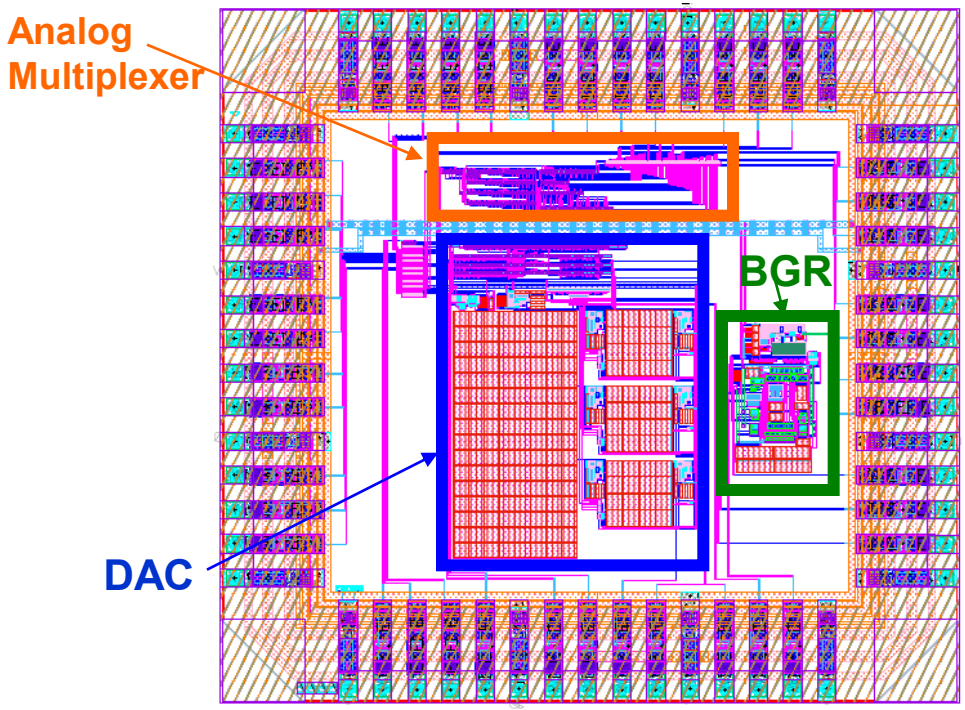


Pipeline A/D Converter test chip



Wilkinson D/A Converter, analog multiplexer, and Bandgap Reference test chip

Example Application – Robotic Arm Control on a System With Distributed Computing

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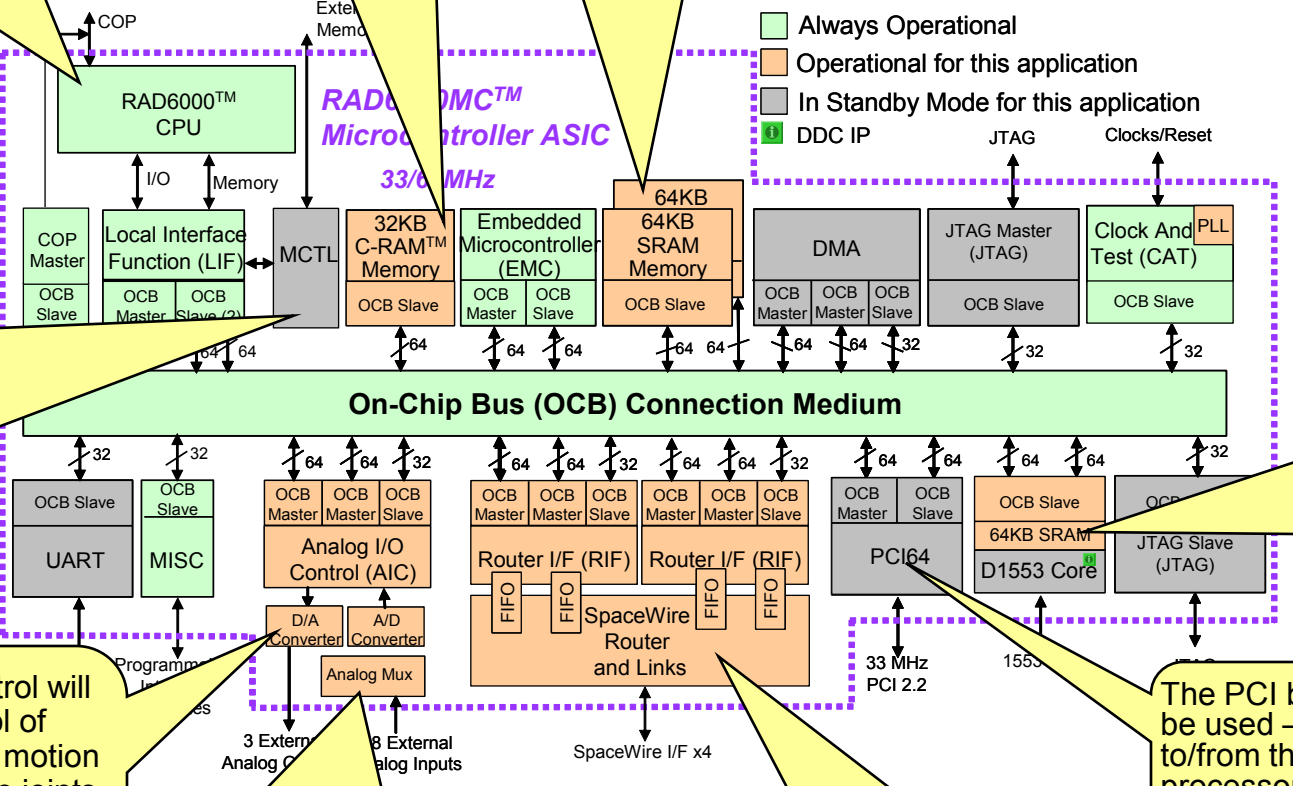
The RAD6000 floating point execution unit will be used to calculate required turning movements

The RAD6000 would be booted from the on-chip C-RAM non-volatile memory

Limited data is collected and stored, so on-chip memory should be sufficient in this case

As a distributed processor with very specific functions, a microkernel Operating System is viable - external memory is probably not required for this application



The 1553 interface is not required so it is shut off, freeing up an additional on-chip 64 KB memory block

Robotic arm control will require control of actuators for arm motion using one or more joints with turn/twist and open/close capability that can be supported by the D/A converters

Tactile feedback for contact and grip pressure use pressure sensors that will feed into the A/D converter through the multiplexer

SpaceWire serial links are used to support high speed data transfers, with routing to other subsystem elements as required

The PCI bus would not be used – transfers to/from the main processor would occur across SpaceWire links

Example Application – Small Satellite Flight Computer

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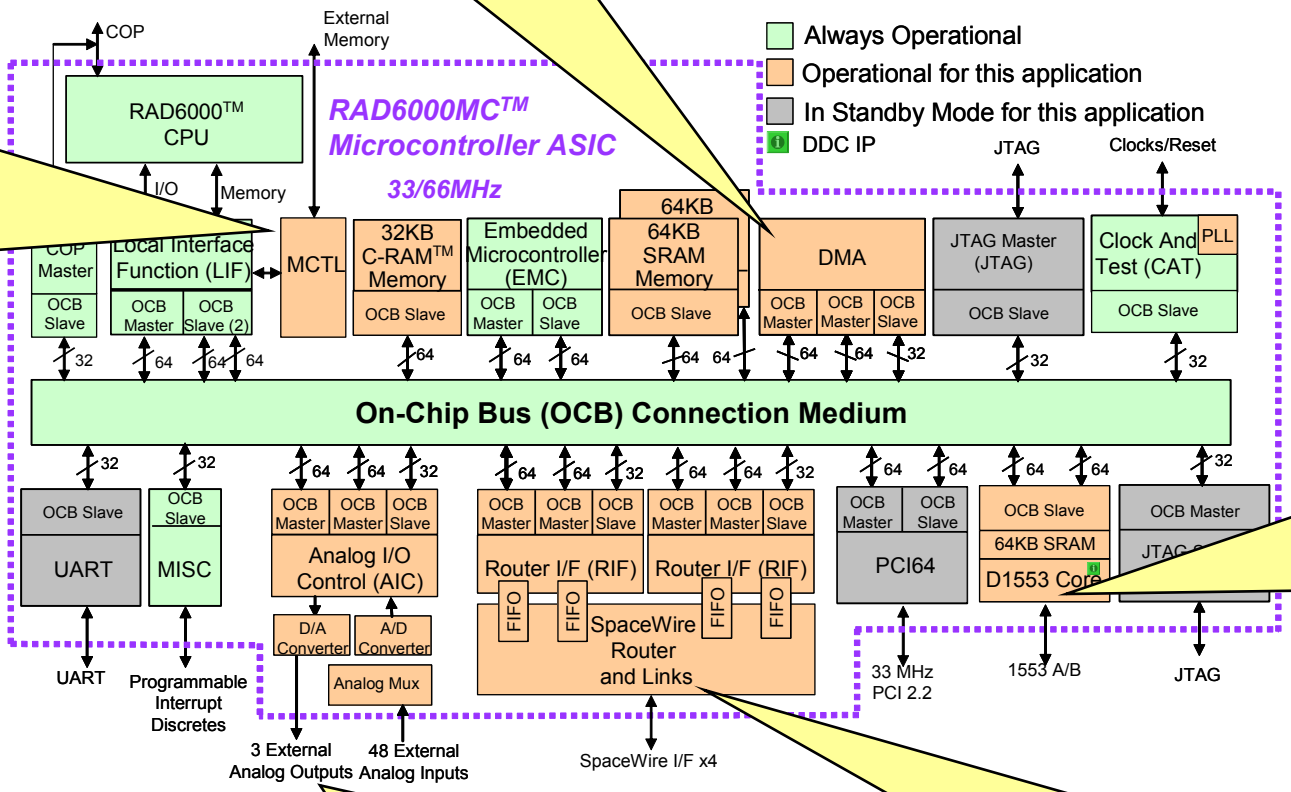
The RAD6000 would run a robust real-time Operating System, necessitating use of additional external memory

The DMA core would perform block memory transfers between on-chip and external memory



1553 bus used for GNC units such as star trackers, inertial measurement units (IMU), and reaction wheels

Analog interfaces will be used in both directions: actuator or thruster control (D/A) and sensor health monitoring (multiplexed A/D), with the EMC assisting in management of collected sensor data to memory

Traffic between subsystems would travel across the SpaceWire links and through the router, requiring operation of the PLL associated with the serial links and the EMC used to control transfers between the router and on-chip memory blocks

Summary

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- The RAD6000MC is a flexible microcontroller supported by a robust set of digital and analog interfaces
  - A redundant MIL-STD-1553 is provided, with embedded SRAM that can be used elsewhere if the interface is not used
  - A SpaceWire router with 4 serial links and dual internal ports is provided for high speed transfer with minimal connections
  - A 64-bit PCI interface offers increased parallel bus throughput
  - Analog/Digital conversion is supported by a programmable multiplexer
  - A novel approach was employed to achieve multiple channels of Digital/Analog conversion with very low power dissipation
- Enhancements have been made to address previous limitations in the RAD6000 microprocessor's addressable memory space
- The ASIC is built around a reusable core architecture and heavily leverages reuse of validated and flight proven designs
- RAD6000MC configuration can be matched to user applications, optimizing features and power dissipation