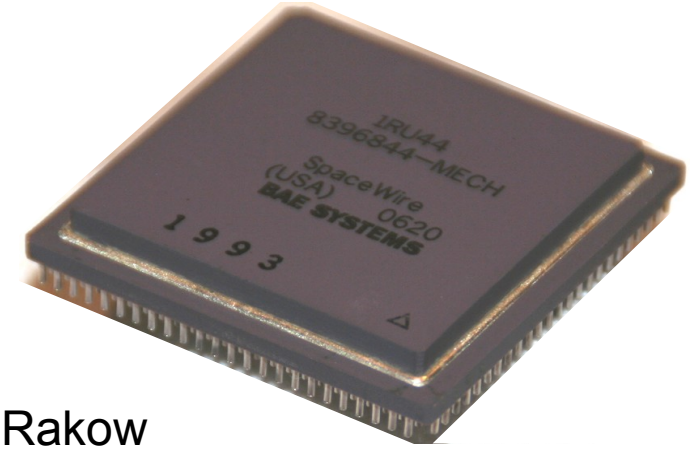
A ONE CHIP HARDENED SOLUTION FOR HIGH SPEED SPACEWIRE SYSTEM IMPLEMENTATIONS



Joseph R. Marshall, Richard W. Berger, Glenn P. Rakow
19 September 2007 – SpaceWire Conference

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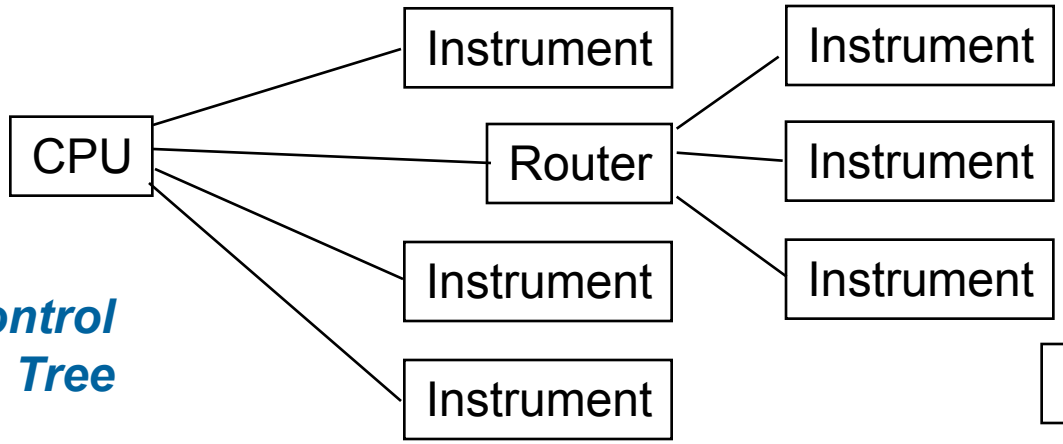
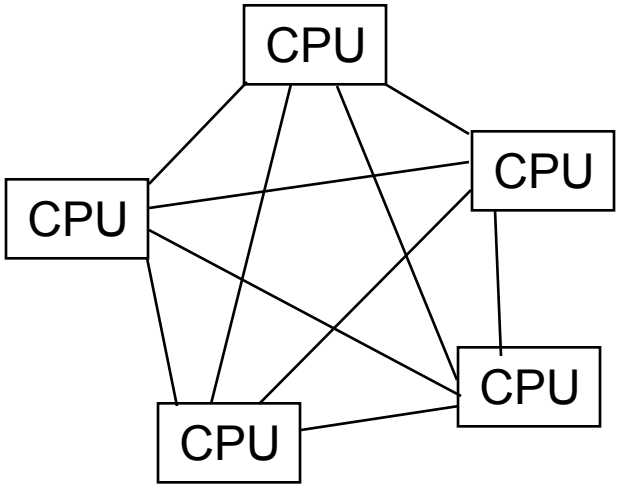
- SpaceWire Boards
- SpaceWire Routers & MCMs
- SpaceWire Product Roadmap

Examples of SpaceWire Topologies

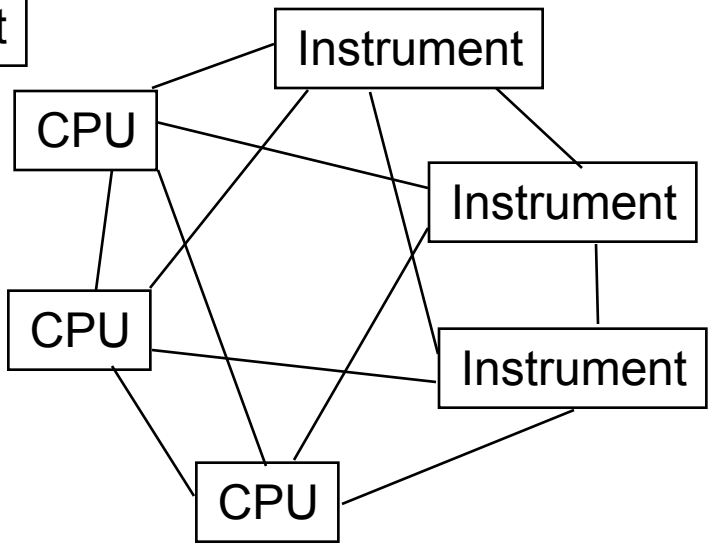


Control Tree



Data Mesh

Rings



The four port router built into the BAE SpaceWire ASIC makes many useful spacecraft topologies possible

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Standards Comparison

Standard	**SpaceWire**	**MIL-STD-1553B**	**1394a**	**cPCI**
Attribute				
Width	Serial	Serial	Serial	32/64
Topology	Point to Point	Bus	Point to Point	Bus
Maximum Frequency	10-264 MHz*	1 MHz	100-400 MHz	33-66 MHz
Maximum Data Rate/Node	212 Mbps*	0.500 Mbps	400 Mbps	1056-4224 Mbps
Maximum Data Rate/Network	27136 Mbps*	0.500 Mbps	400 Mbps	1056-4224 Mbps
Maximum Nodes	256 (Unlimited)*	32	63	8 to 4
Isolation between Nodes	LVDS	Transformer	Galvanic	Resistor
Node Redundancy	Full Port	PHY Only	PHY Only	Device

**Based on BAE Systems Implementations*

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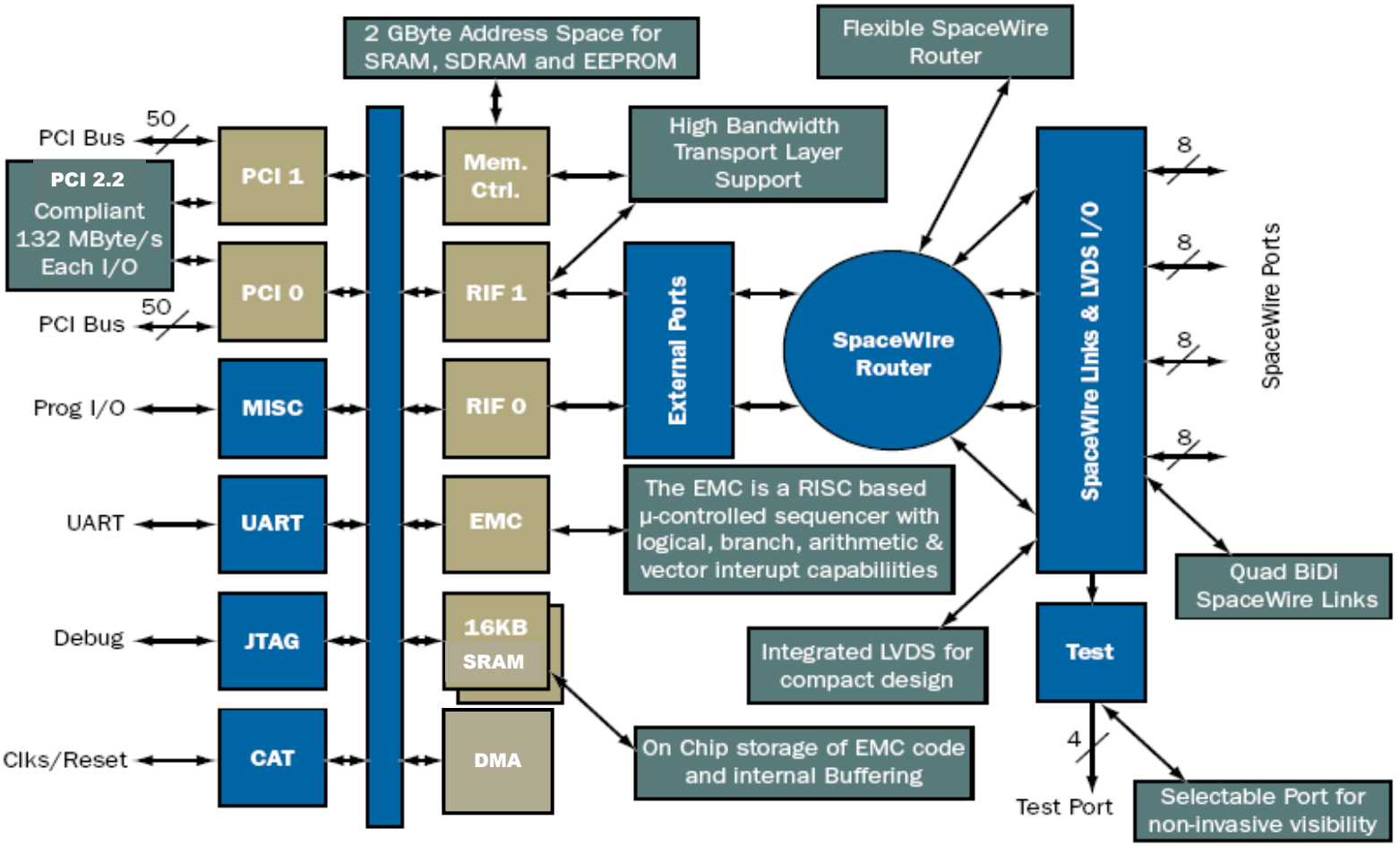
BAE Systems SpaceWire ASIC Program

- Program initiated in March 2003
- BAE Systems and Goddard Space Flight Center (GSFC) joint development effort
  - Modeled in VHDL
  - 250nm CMOS technology ASIC
    - 2.5V core supply
    - 6 layers of metal
    - Flip-chip mount to package
  - Based entirely on synthesizable cores
    - Reused BAE Systems cores and On Chip Bus connection medium
    - Reused GSFC SpaceWire router core with extensions for transport layer support and dual external interfaces
    - New interface between router and On Chip Bus
- Design was funded by Glenn Research Center
- Design Changes, manufacturing and test was funded by GOES-R mission
  - First hardware in 4Q 2005
  - Flight Qualification testing complete
  - Flight modules available

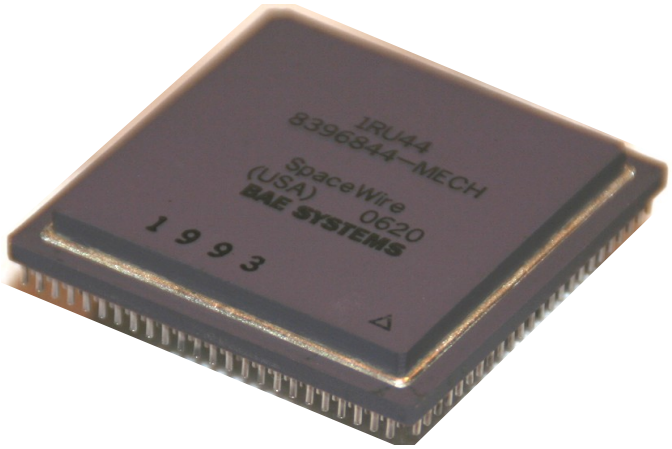
4 Port SpaceWire ASIC Block Diagram

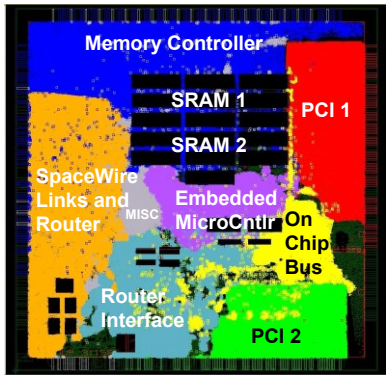


4 Port SpaceWire ASIC

- **SpaceWire Interface**
  - 6 port switch
    - 4 SpaceWire serial ports (addresses 1-4)
    - 2 local parallel ports interface to the On Chip Bus via a Router Interface (RIF) core (addresses 5-6) providing higher throughput and minimizing risk of bottlenecks
    - Configuration port is address 0
  - SpaceWire ports include internal LVDS drivers / receivers with support for cold sparing
  - 264 MHz maximum data rate on SpaceWire link interfaces
- **Dual PCI ports (version 2.2)**
  - Up to 66 MHz operation
  - 32-bit address / data bus
  - Parity and cold spare
- **Memory interface w/error correction**
  - Supports EEPROM, SDRAM, SRAM
  - Single bit / nibble error correction
- **Embedded Microcontroller**
  - Internal 32 KB SRAM and DMA Controller
- **Test interfaces**
  - 16550 UART
  - JTAG
  - SpaceWire test data (SNIF) access port
- **Packaging *(TRL-9)***
  - 32mm 624 pin ceramic CGA
  - 423 of 504 signal pins used
- **Low power**
  - 3.3V I/O & 2.5V core supplies
  - 1-4 W depending on speed and usage

- **Radiation hardened R25 library and technology *(TRL-9)***
  - 200 Krad(Si) Total Dose
  - <1E-9 upsets/bit-day SEU
  - Latch-up immune
  - SEU-hardened RAMs, flip-flops, clocks

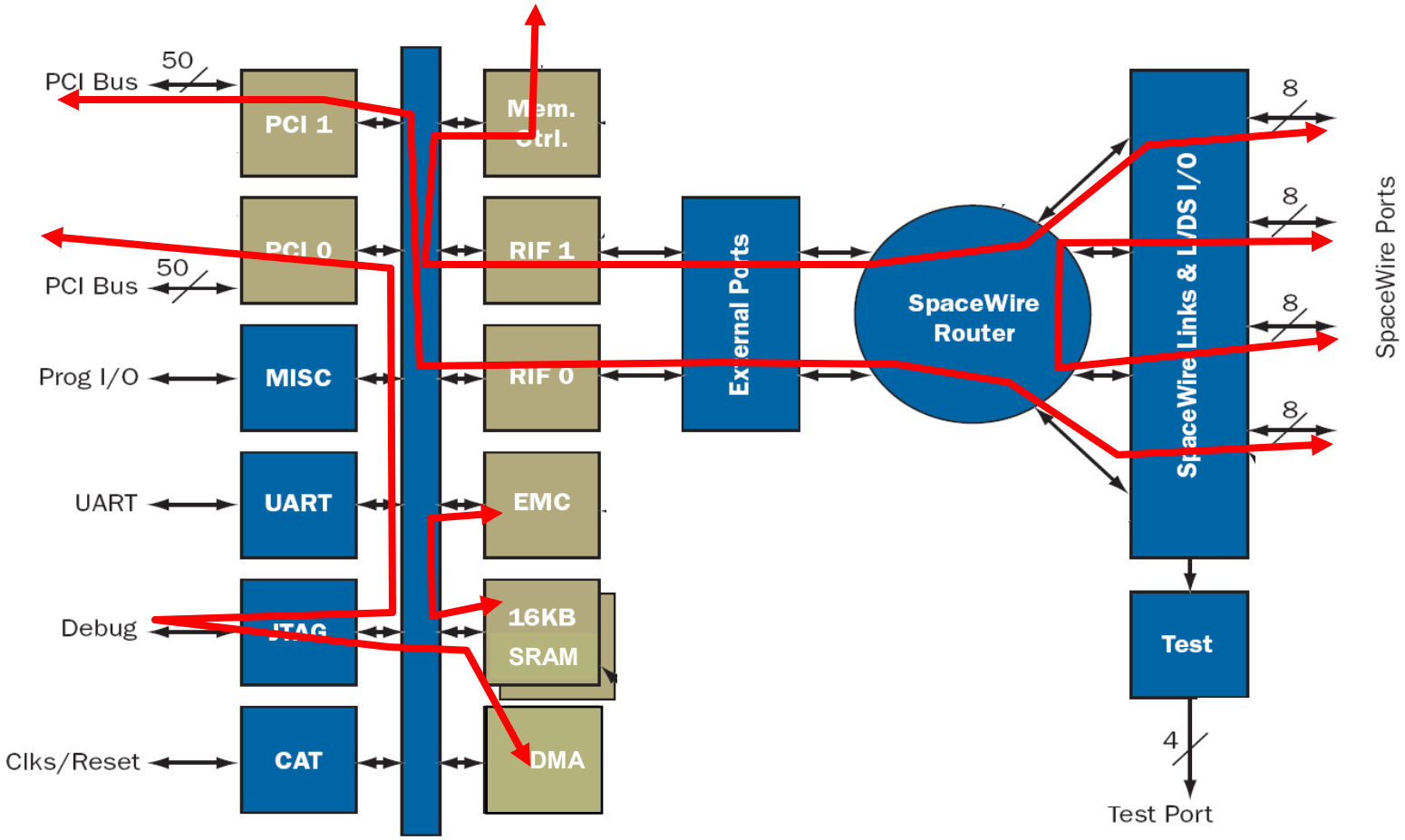




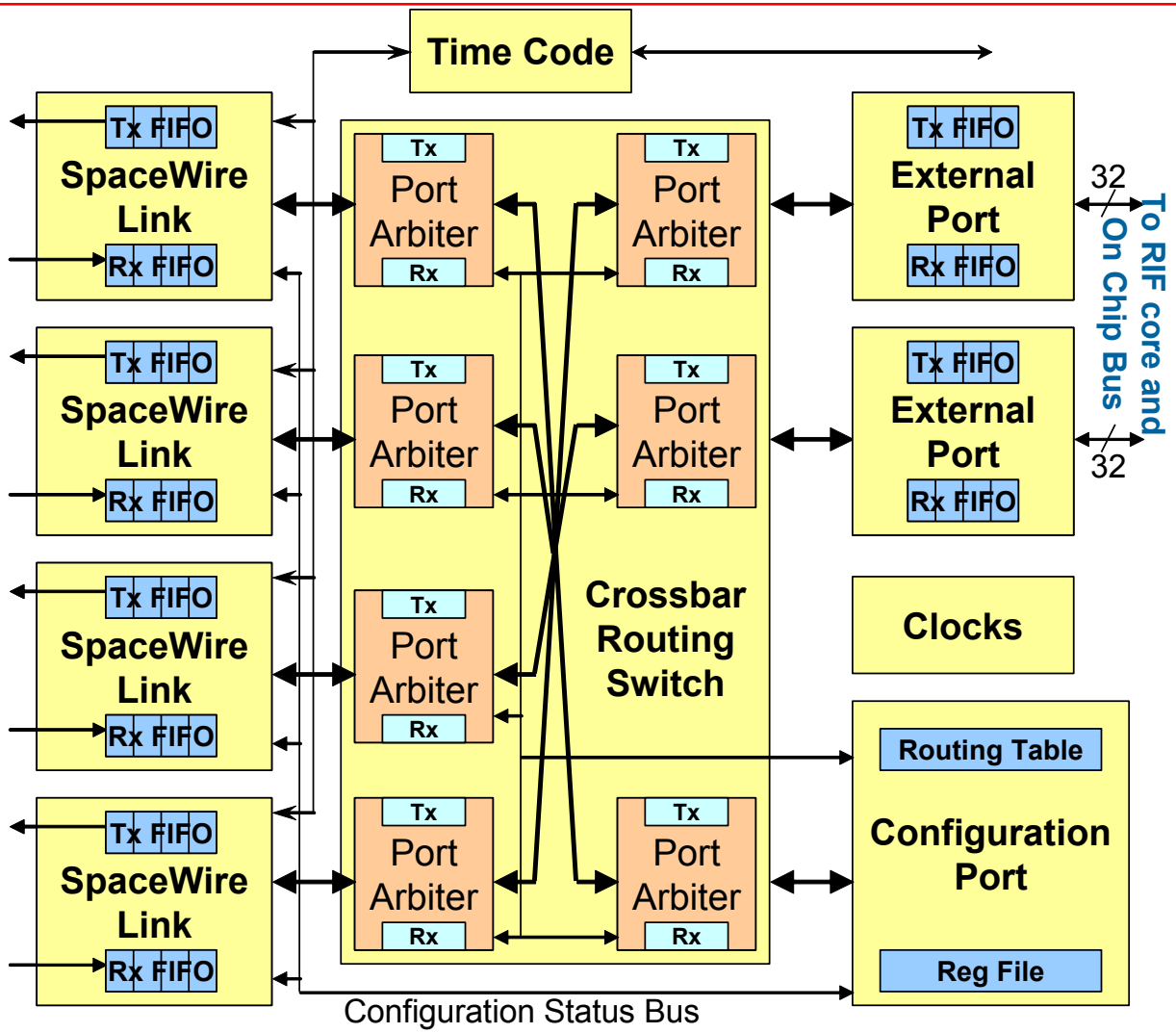
12.7mm x 12.7mm die

Flight parts and boards are being delivered to multiple space missions

Simultaneous Paths through SpaceWire ASIC

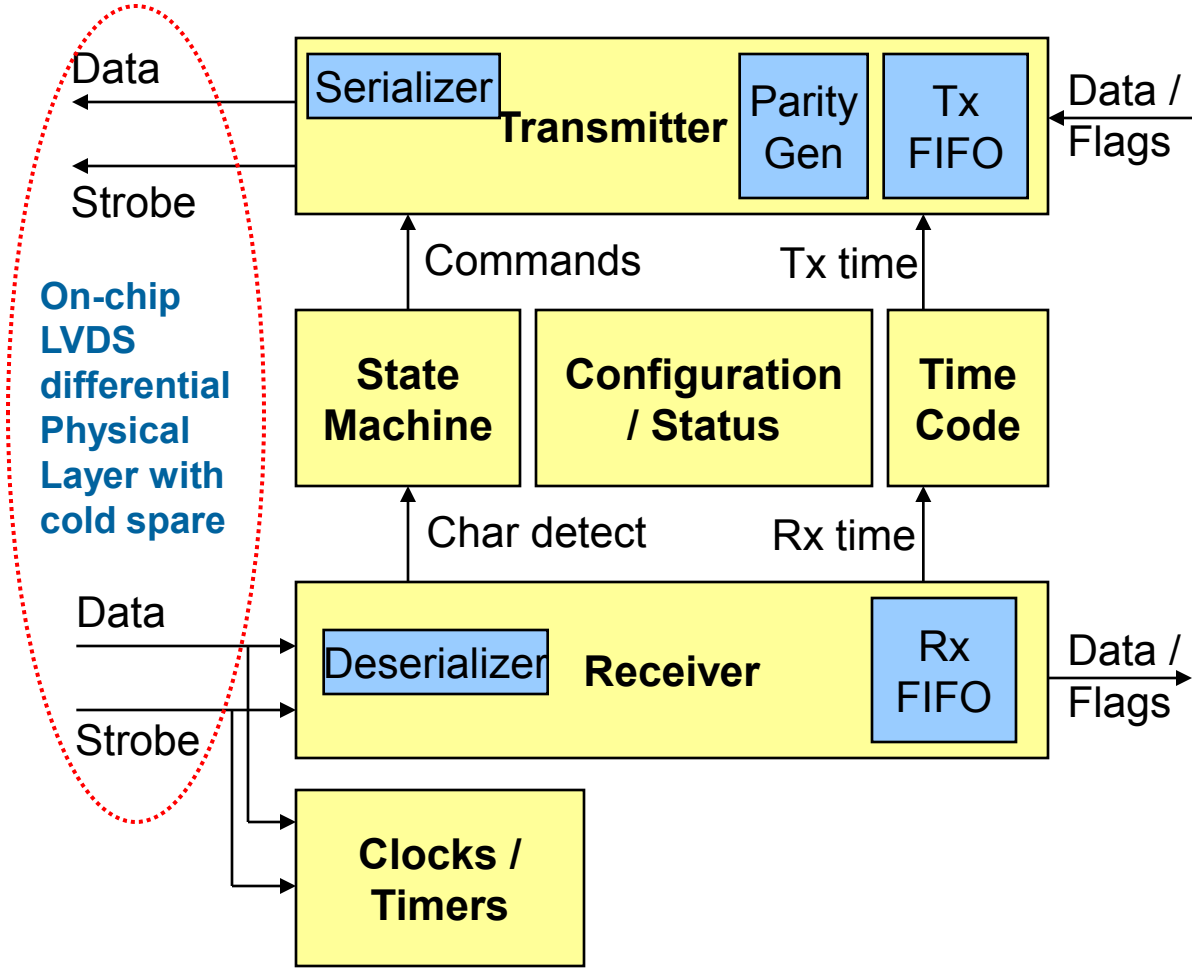


SpaceWire Router Implementation



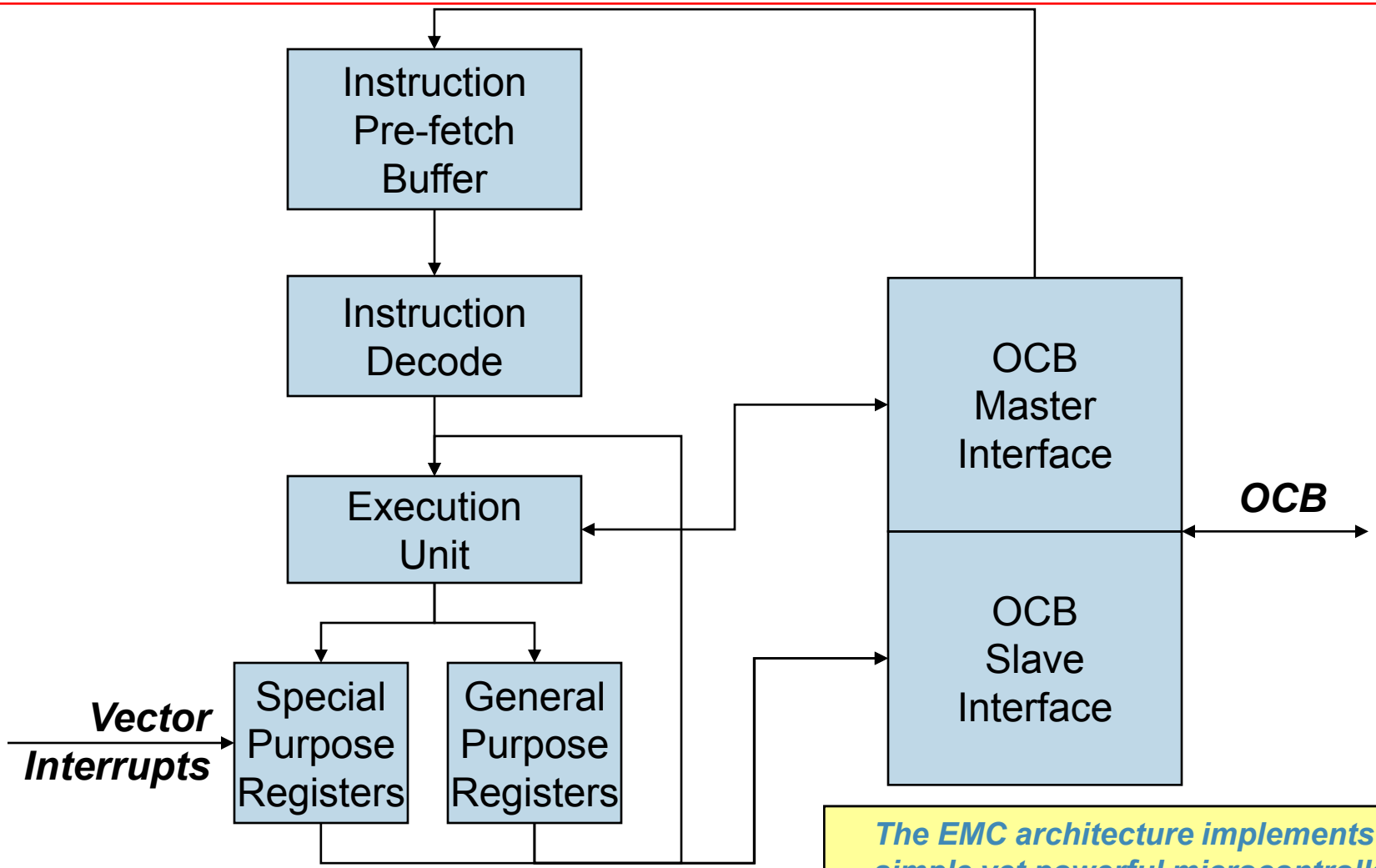
- The router is a non-blocking crossbar switch
  - **Employs non-prioritized, round robin arbitration for output port access upon contention**
  - **Router can limit maximum packet size**
- The router switch implements a port arbiter on each port, each of which has a Tx arbiter and Rx requester
- Bypass mode with local header that defines arrival port and presence of logical address

SpaceWire Link Port Implementation



- **Variable SpaceWire data transfer rate**
  - **Controlled by 6-bit rate field**
  - **Generated from Tx clock**
  - **Power-up initializes to 10MHz**
- **The receive clock is recovered by XORing data and strobe signals**
- **The clock block generates the 4x link interface clock via Phase Locked Loop (PLL)**
- **Tx and Rx FIFOs are 64 words deep by 32 bits wide**
- **LVDS drivers and receivers are instantiated on the chip and support cold sparing**

EMC Core Block Diagram



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Embedded Micro-Controller (EMC)

- Handles Reset of RAD750
- Handles Critical Errors to Keep CPU Out of Checkstop
- Part of Bridge ASIC for RAD750 (Power PCI)
- Also Part of SpaceWire Bridge
- Expanded General Purpose Registers and Instruction Set
- Full Access to Bridge Resources
- Instruction Cache
- One Enhancement Cycle Complete (Enhanced Power PCI)

The EMC takes full advantage of the rich functions of its bridge and the high performance connections to each

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Software – EMC Tool Chain Overview

- The EMC Tool Set allows the development of ANSI-C code targeted for the EMC. It consists of the following tools:
  - Lcc compiler targeted for the EMC (consists of a pre-processor and compiler)
  - EMC assembler built on top of the GNU assembler PPC "GASM"
  - The GNU linker to link EMC C and assembler code.
  - EMC Map to extract binary and debug information from output of GNU linker.
  - EMC Debugger for source level debugging of C & assembler code:
    - On target ASIC via JTAG
    - With EMC Simulator (simulation of EMC instruction set and memories)
- Toolset has been in use since 10/2005
- Previous Assembler-only toolset used since 1/2000 for RAD750 SUROMs

These tools enable applications to be built and simulated in high level language environments

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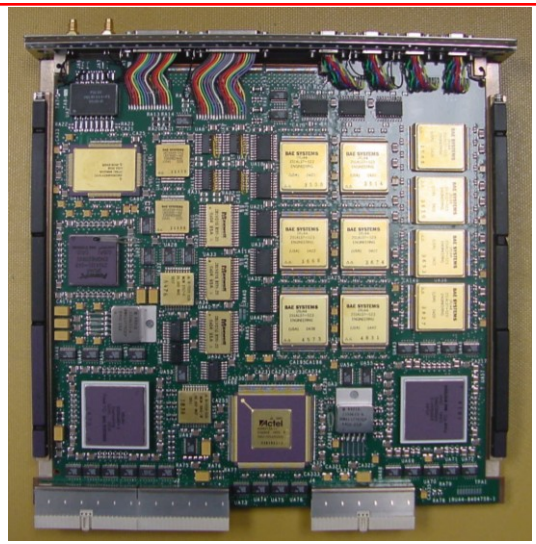
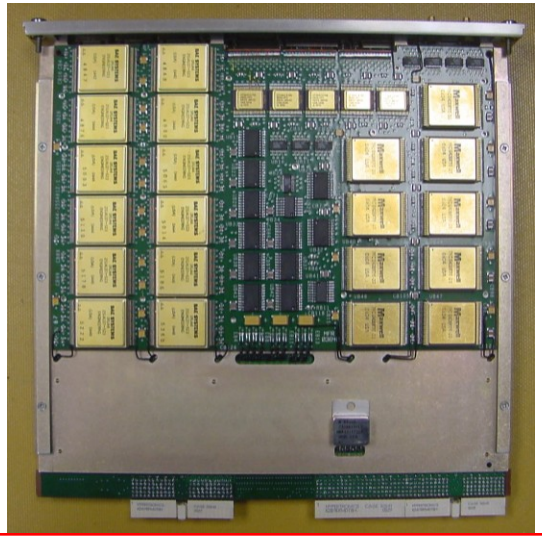
SpaceWire Boards

- LRO SBC Board – 6U 220 RAD750 Single Board Computer
  - 4 SpaceWire Ports + Memory + 1553
- LRO Application Board – Custom Slice RAD750 Single Board Computer
  - 4 SpaceWire Ports + Memory + 1553
- UFSD Test Board – Reconfigurable Processing Board
  - 4 SpaceWire Ports + C-RAM Memory + Xilinx FPGA + FRED + Rocket I/O
- Customer Evaluation Board – 6U 160 SpaceWire CompactPCI Board
  - 4 SpaceWire Ports + Memory

4 Port 6U-220 RAD750/SpaceWire/1553 SBC

- **External Interfaces**
  - Backplane Interfaces;
    - 33MHz PCI Bus in CompactPCI compatible format
      - Operates as Central Resource
      - Supports up to five other PCI Bus Masters or Slaves.
    - Provides up to 27 single ended discrete input,
      - discrete output or interrupt input signals
  - Four SpaceWire Interfaces, each capable of operation at up to 264 MHz.
  - MIL-STD-1553B Bus A & Bus B interfaces; Operates as either BC or RT
  - Provides four RS-422 discrete inputs and four RS-422 discrete outputs.
    - Also provides an RS-422 watchdog timer expired output.
  - Test interface containing JTAGs and UART for ground level debug
- **Capabilities**
  - RAD750 PowerPC 750 running internally at 132 MHz and externally at 66 MHz
  - En-Power PCI & SpaceWire contain Embedded Microcontrollers running at 66MHz
  - Six 32-bit programmable up/down timers; Four of these can be externally operated.
  - Multiple DMA Controllers – contained within the En-Power PCI, SpaceWire and SPIF
  - Local Memory EEPROM can be powered off while the LRO En-SBC remains active.
- **Capacities**
  - Local Memory SRAM = 36 Mbytes plus SECDED error correction code (ECC)
  - Local Memory EEPROM = 4 Mbytes plus SECDED ECC
  - SpaceWire SRAM = 8 Mbytes plus SECDED ECC
  - SUROM = 64Kbytes (PROM) or 256Kbytes (EEPROM) plus SECDED ECC
  - 1553 SRAM = 64Kbytes
- **Characteristics**
  - Operates from +3.3V and +5.0V supplied at backplane;
    - Requires proper voltage sequencing.
  - Operating Temperatures: -20°C to +50°C
  - Power consumption (est.): Maximum of 21.4 Watts for LRO usage.
  - Card envelope: Height=40.64mm, Width=231mm, Length=220mm.
  - Weight (est.): 3.790 lbs (1.723 kg)





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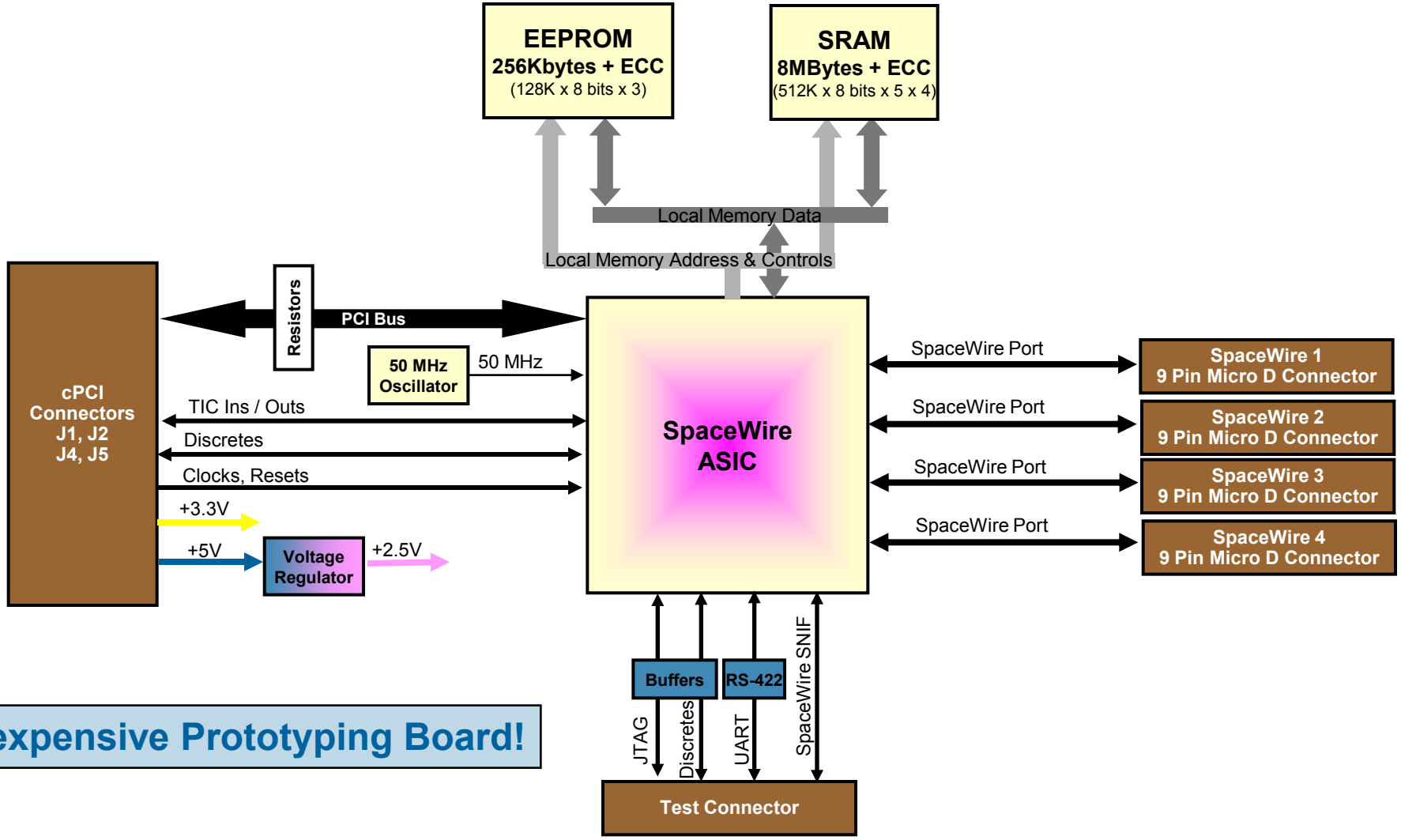
Software Support for SpaceWire ASIC

- Supporting software development
  - On-chip Embedded Microcontroller (EMC) controls transport layer
  - BAE Systems developed a C compiler for the EMC
  - GSFC is developing code for the EMC
- SpaceWire ASIC device driver written in C
  - RAD750 processor supports all functions via the PCI bus
  - Driver glues together software modules for Programmable Interrupt Discretes (PID), interrupt routing, PCI and address translation, DMA controller, the Router Interfaces (RIF), and SpaceWire router configuration
- Network routing layer on top of device driver
  - Provides queues in the system for incoming packets
  - Used by the LRO C&DH unit
- SpaceWire driver also written on on-chip EMC in C code
  - The EMC generates control block “descriptors” to partition large files into more easily transmittable pieces
  - Requires approximately 40% of EMC throughput capacity

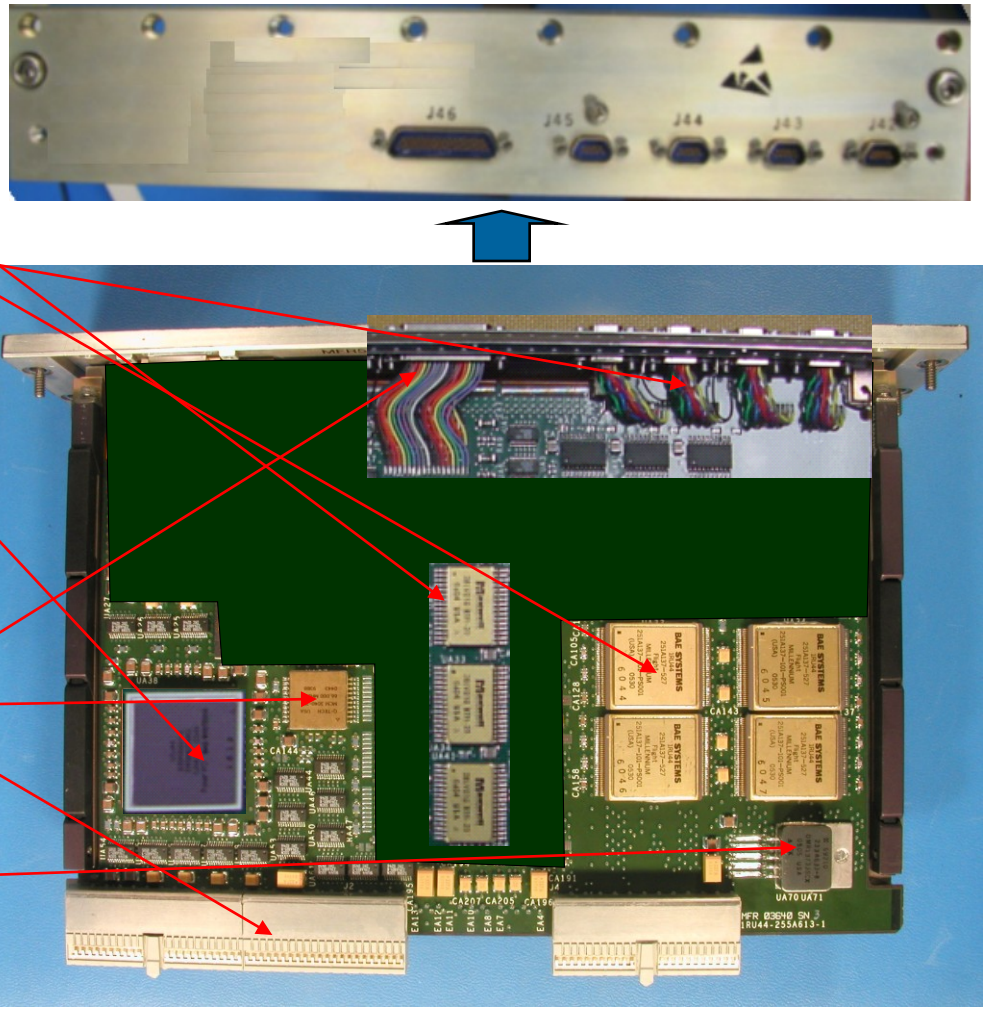
4 Port SpaceWire 6U cPCI Evaluation Board



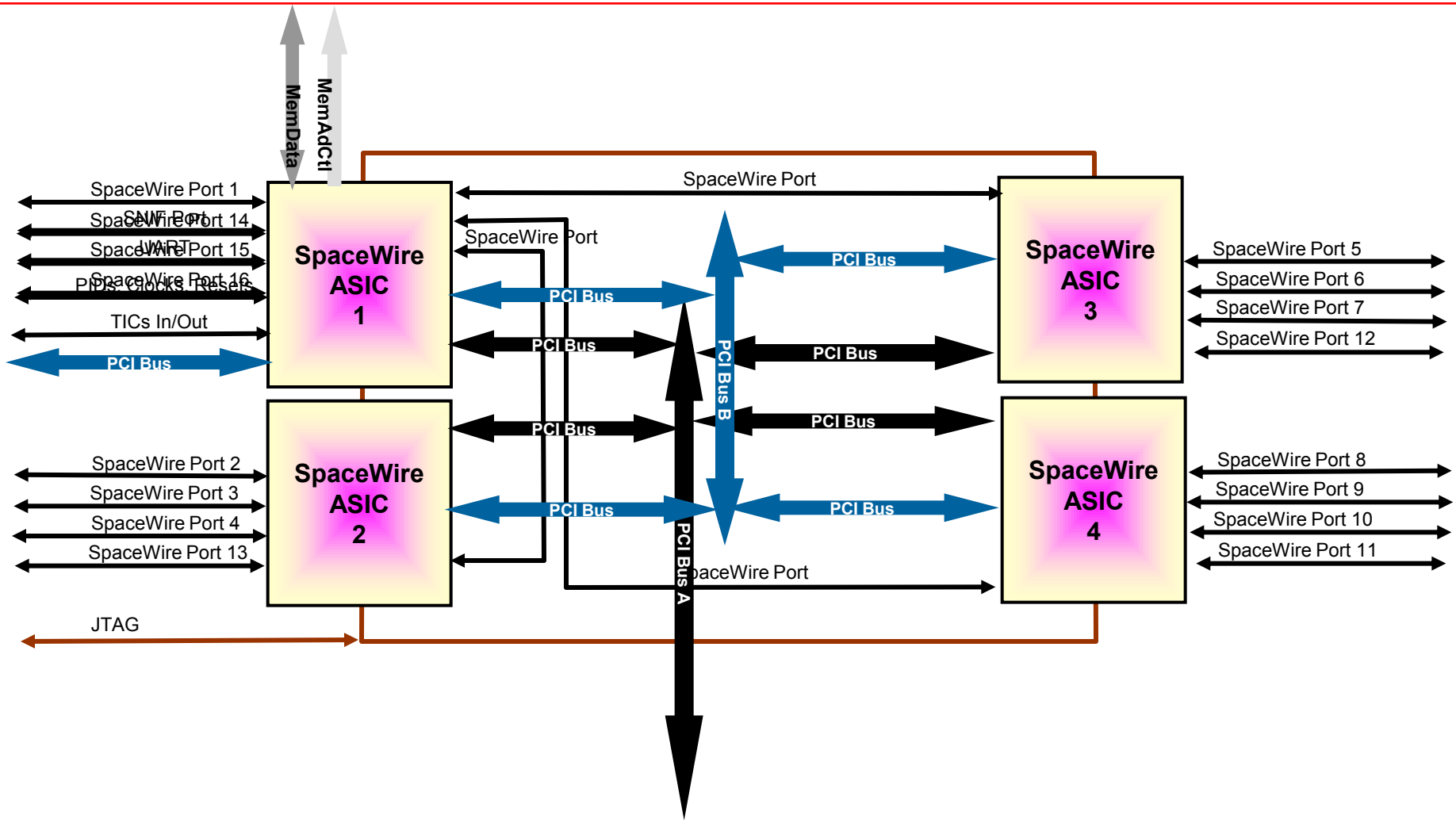
Inexpensive Prototyping Board!

4 Port SpaceWire 6U cPCI Evaluation Board

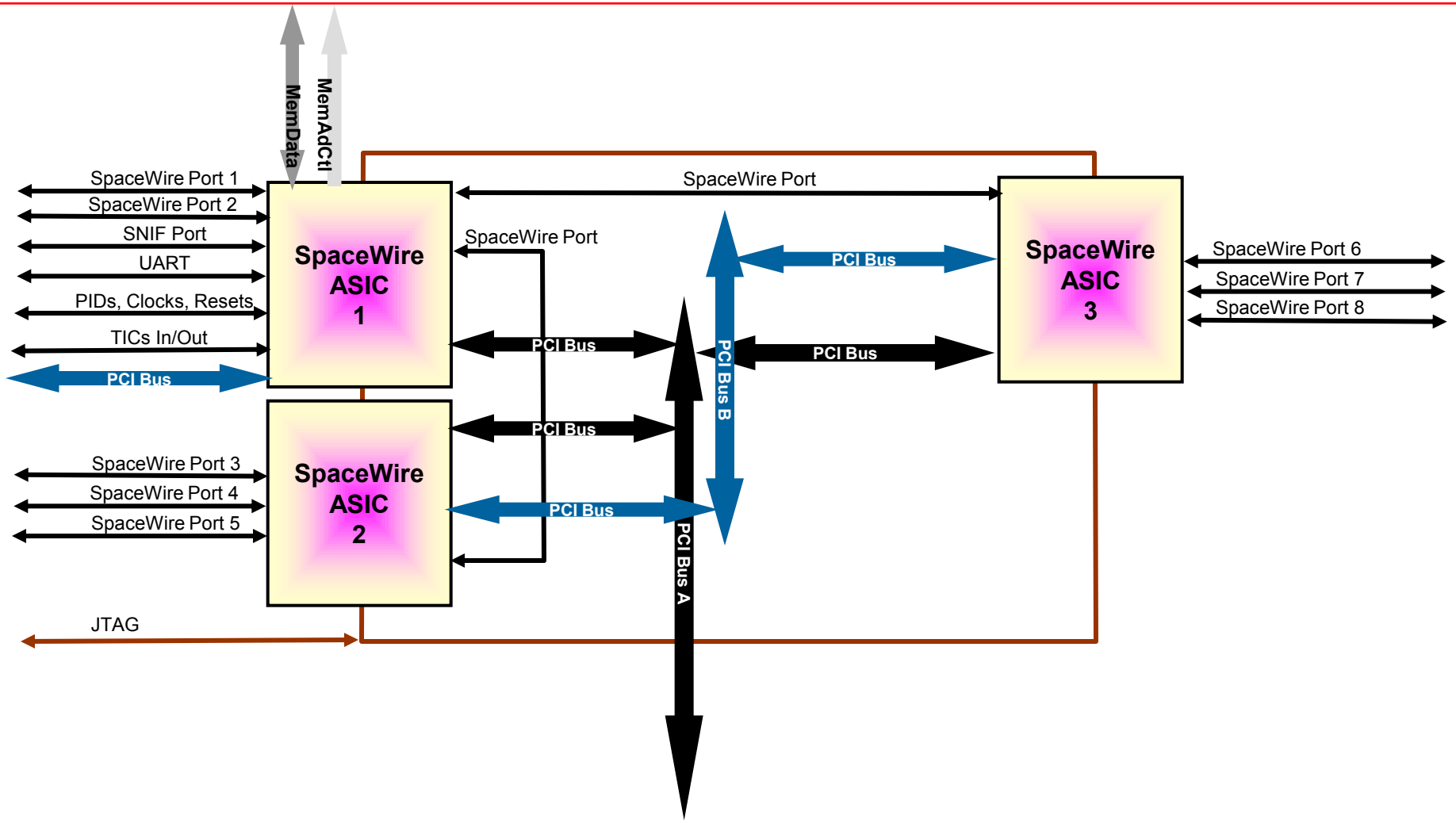
- 256 KB COTS EEPROM
- 8 MB BAE Lab SRAM
- 4 Port SpaceWire ASIC
  - 4 SpaceWire Ports
  - 6 Port Internal Router
  - DMA Controller, 16 MB SRAM
  - Embedded Microcontroller
  - UART
  - JTAG Input, Discretes and Timers
- 6U-160 CompactPCI
  - 32 bit 33 MHz PCI
  - Discretes
- 50 MHz Oscillator
- External Oscillator Input
- 5V and 3.3V Operation
  - 2.5V Regulator on Board
- Test Connector
  - UART, JTAG, Discretes, SNIF Port



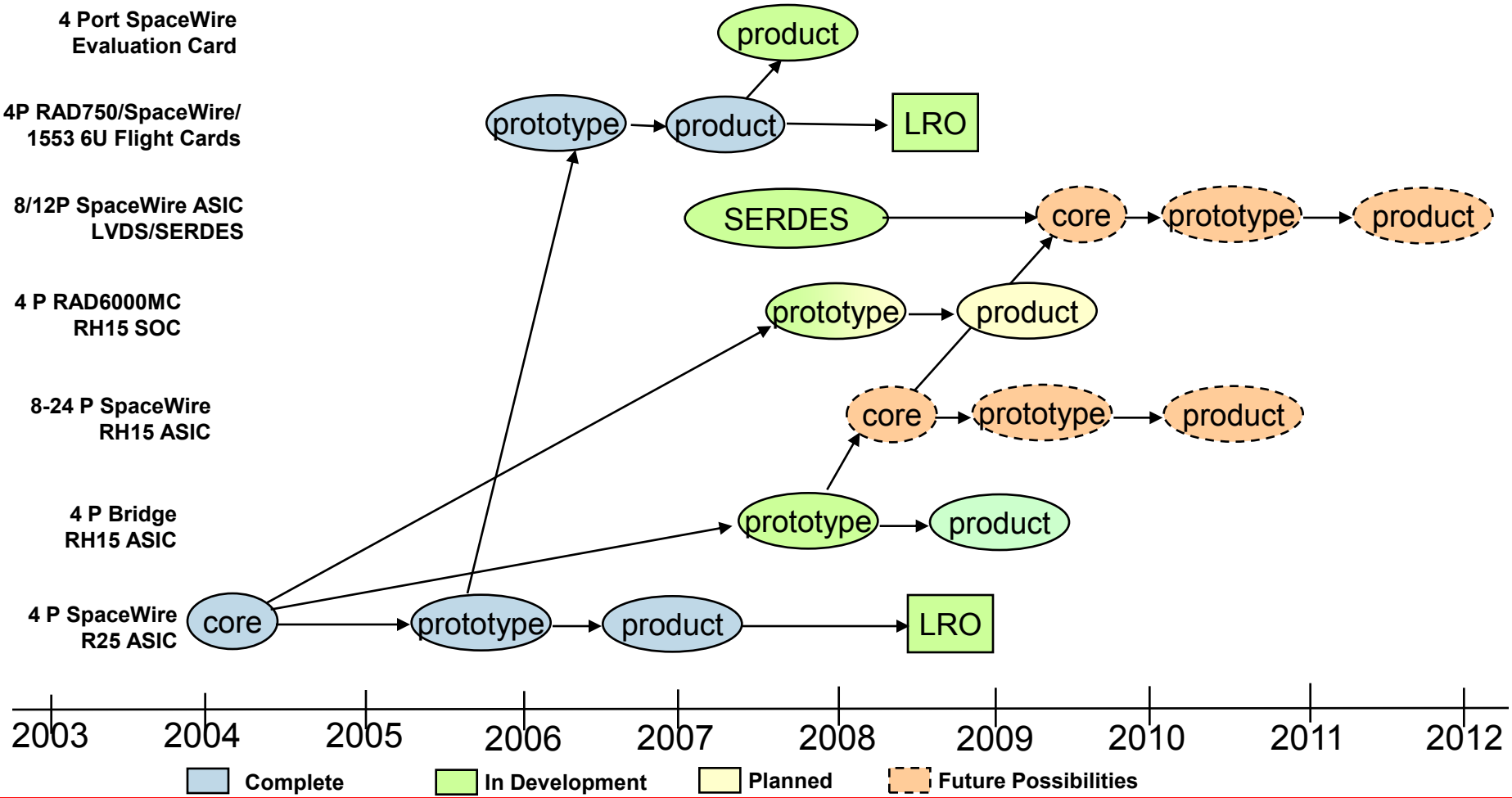
10 Port SpaceWire Hi Perf Router



8 Port SpaceWire Hi Perf Router



SpaceWire External Product Roadmap



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Summary

- Existing SpaceWire Chip built from GSFC and BAE IP
- 4 Ports plus 7 port internal router
- Radiation Hardened and Flight Qualified – will fly in 2008
- Three Board Designs to Date with Evaluation Board by YE2007
- Various Performance Routers may be Implemented
- Full Roadmap for current and future products.

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