Application of SpaceWire to Future Satellite Data Processing System

Kenji Matsuda, Kazunori Masukawa, Shigeru Ishii,
Yo Watanabe, Yoshikatsu Kuroda (MHI),

Motohide Kokubun, Masanobu Ozaki, Tadayuki Takahashi (JAXA),

Masaharu Nomachi (OSAKA UNIV.)

17-19 September 2007
International SpaceWire Conference 2007 @ Dundee, UK

MITSUBISHI HEAVY INDUSTRIES, LTD. (MHI)

JAXA

OSAKA UNIVERSITY

Agenda

(1) Big concerns in development of satellite

(2) Why? How to resolve?

(3) One proposal

(4) Benefit

(5) Summary

Big concerns in managing development of satellite

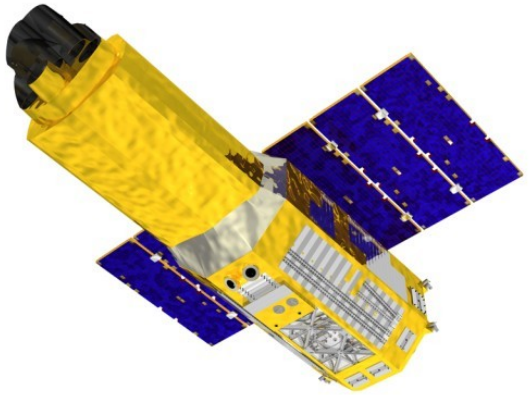
Development period

Cost

Human resource

Quality

etc…



©JAXA

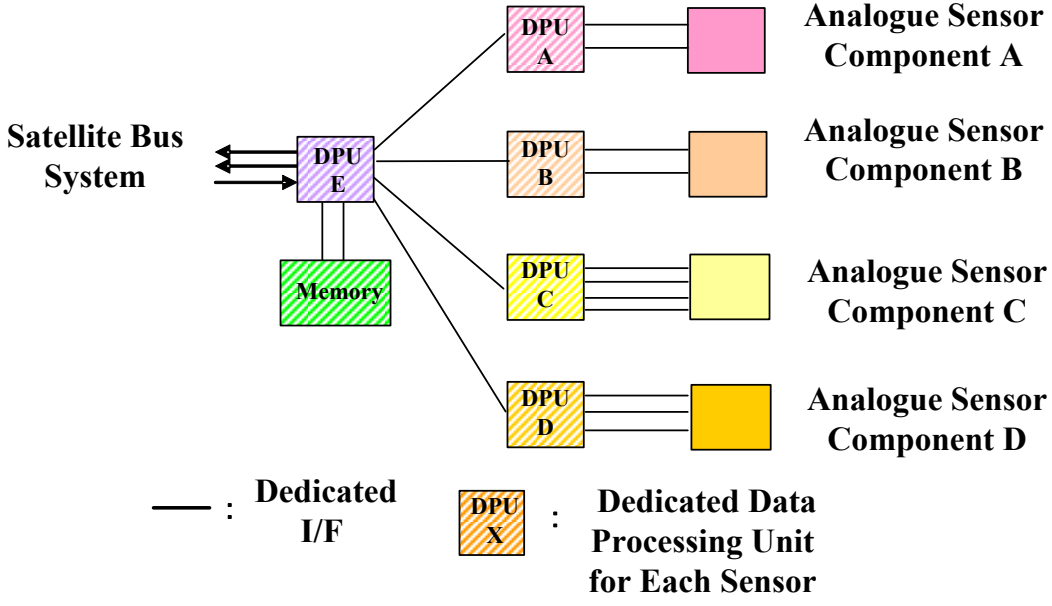
How to reduce the risk ?

For the best performance, many types of DPU (Data Processing Unit) and communication protocol

To design, manufacture and verify…

Many types of DPU

Communication protocol for each line



The basic concept to resolve the issue is
to standardize as many component as possible

HARDWARE

and

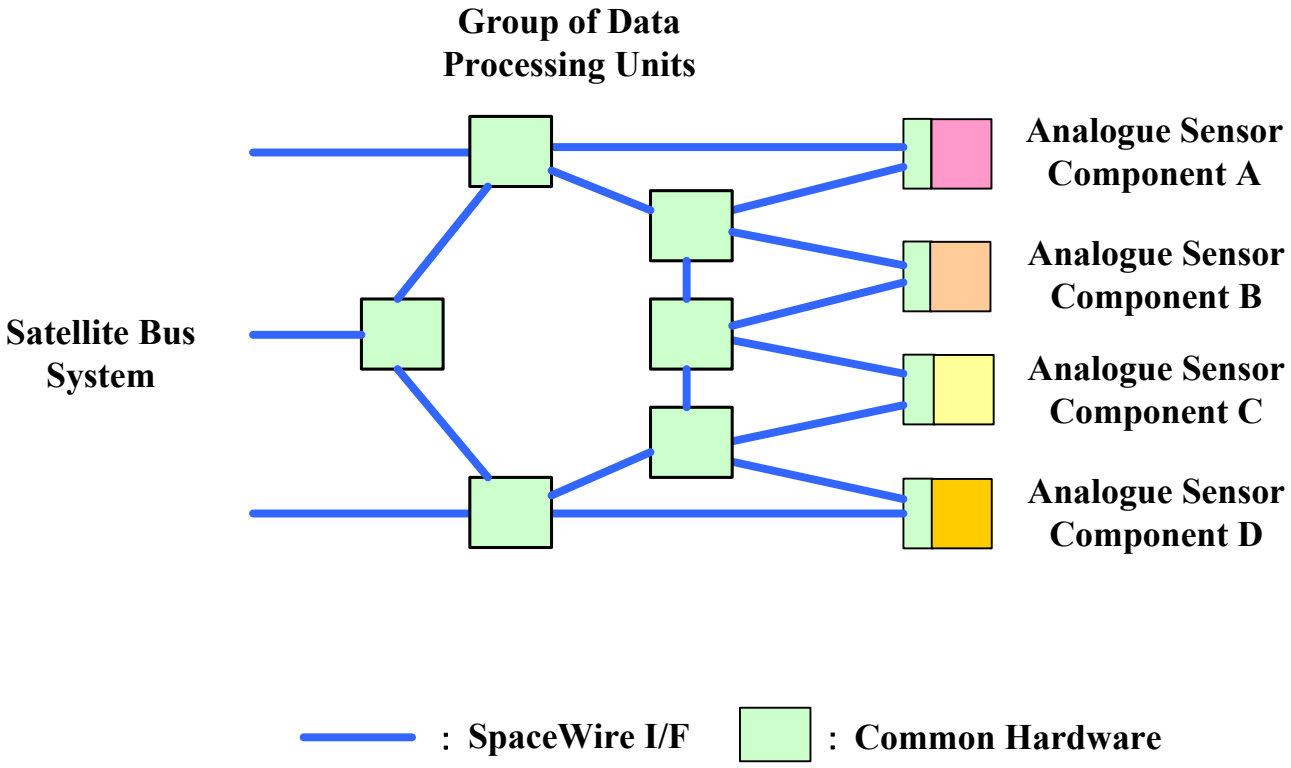
SOFTWARE

MHI's proposal in developing satellite

- To use SpW protocol as the only one protocol
- To develop common hardware
- To link DPU together
- To use TRON-OS

Overall system (1)

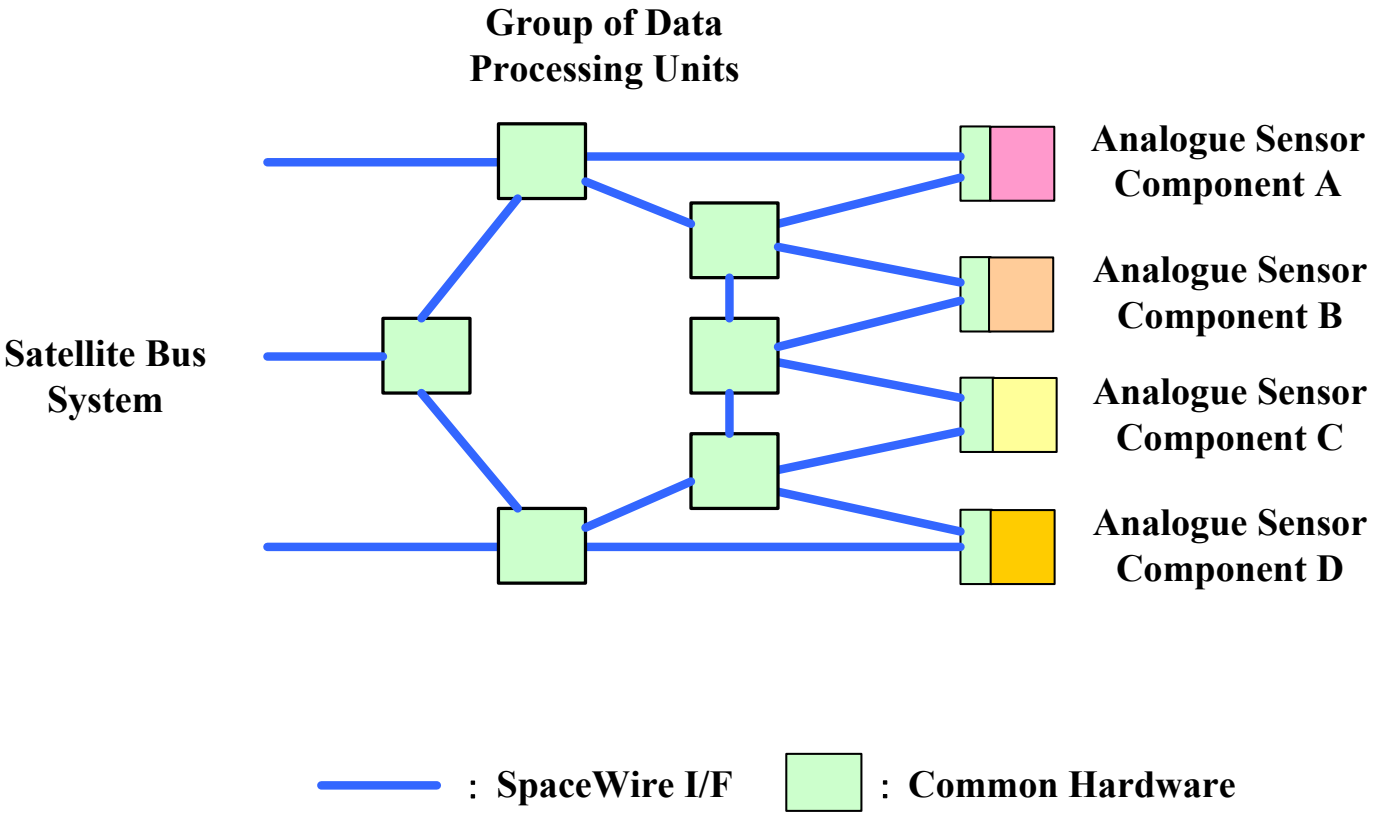
- All protocol is SpW
- The same hardware (SpW Card) is used for each DPU to reduce risk and cost



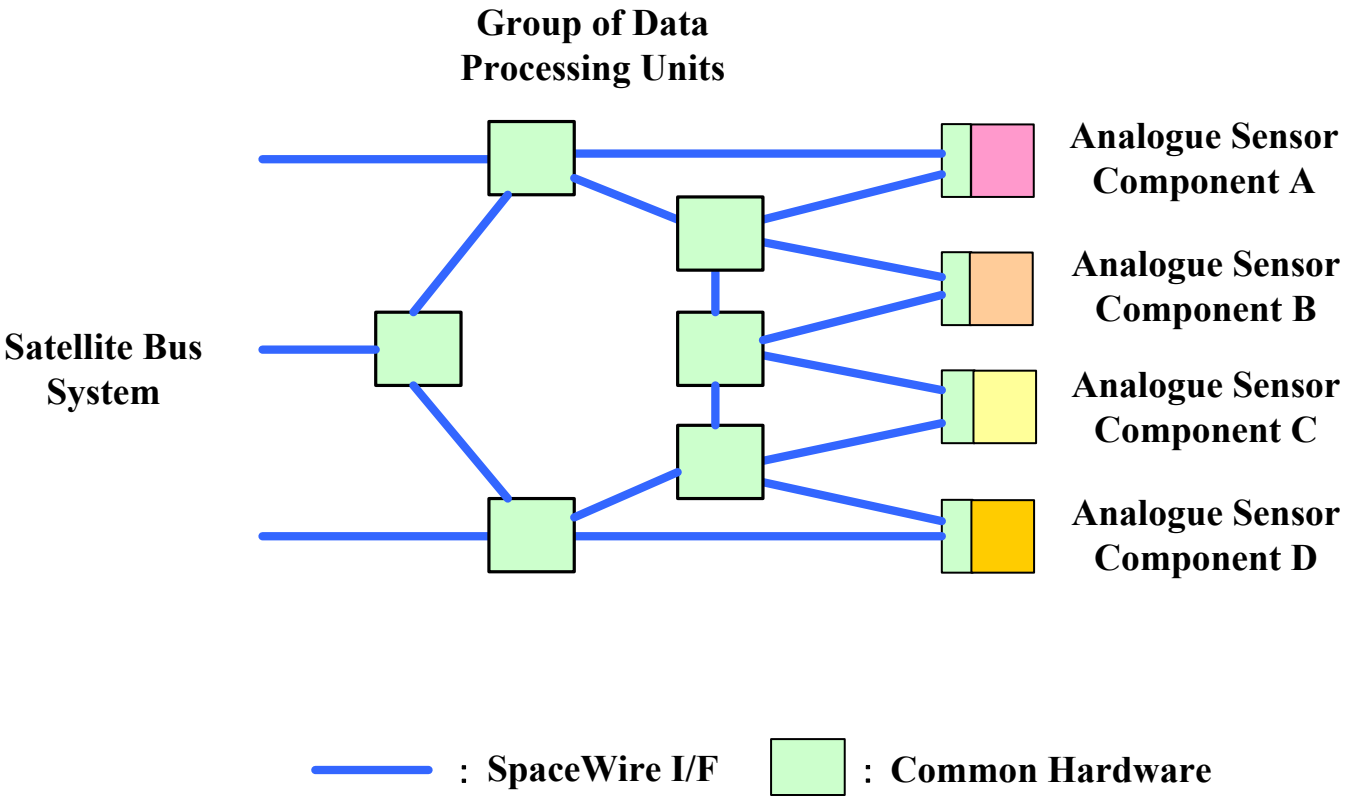
Overall system (2)

To link DPU to form a ring (ring topology)

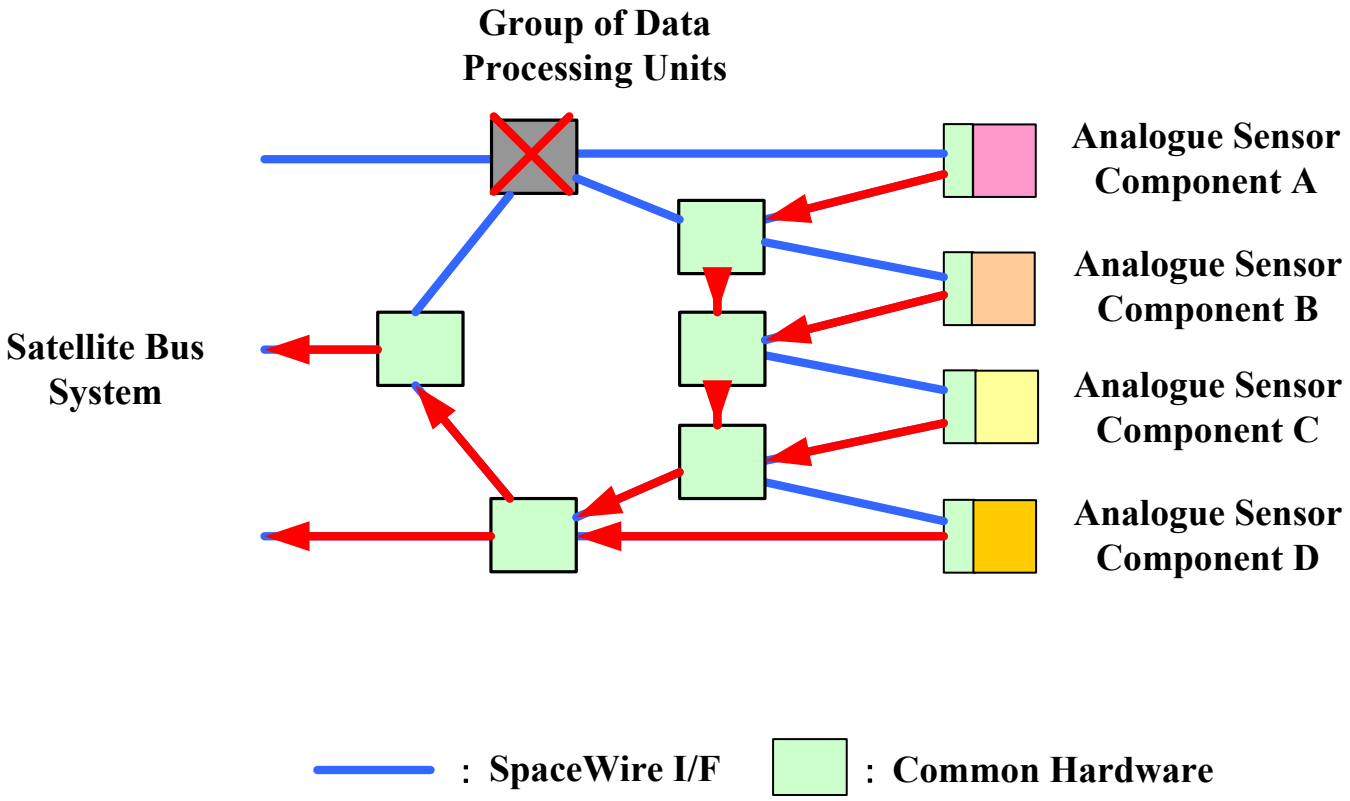
Add at least one DPU as redundancy for fault-tolerance



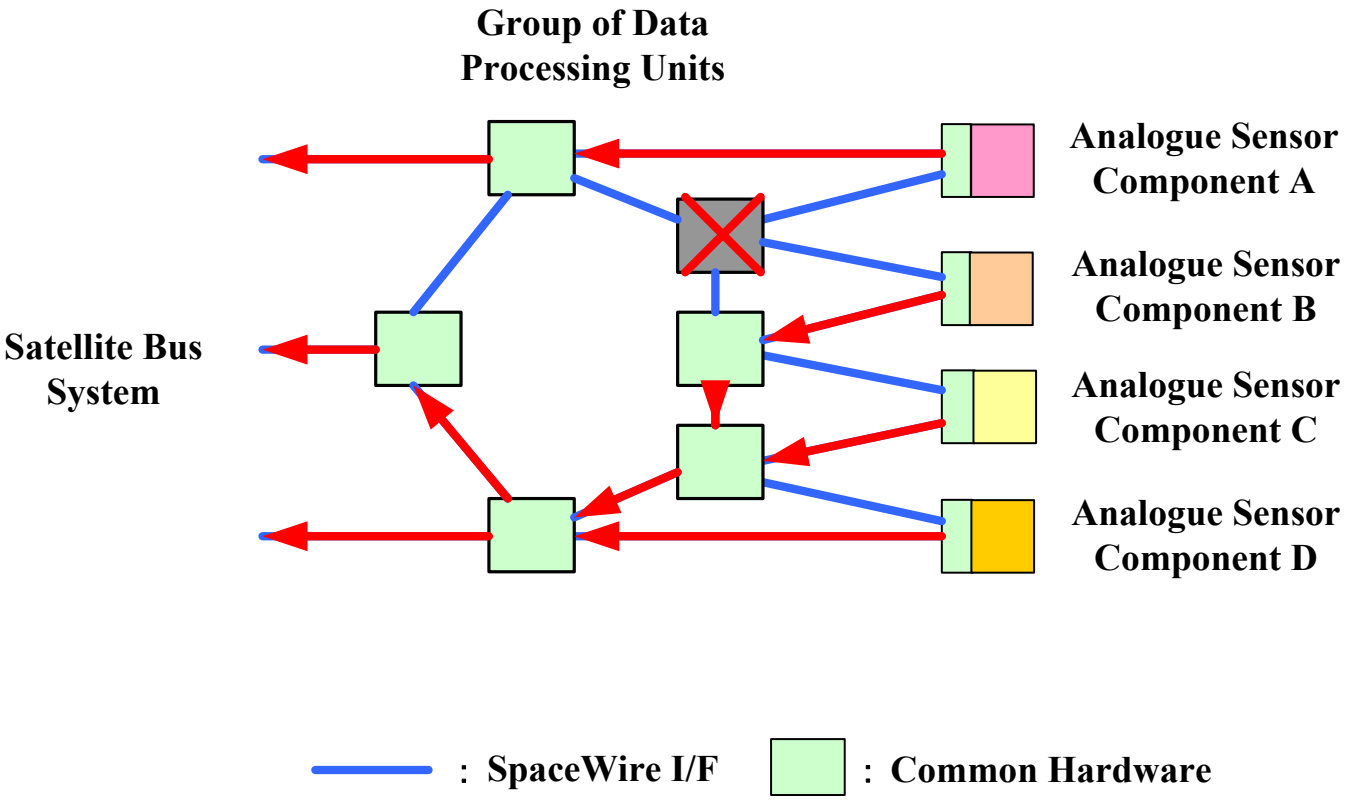
An example of fault-tolerance



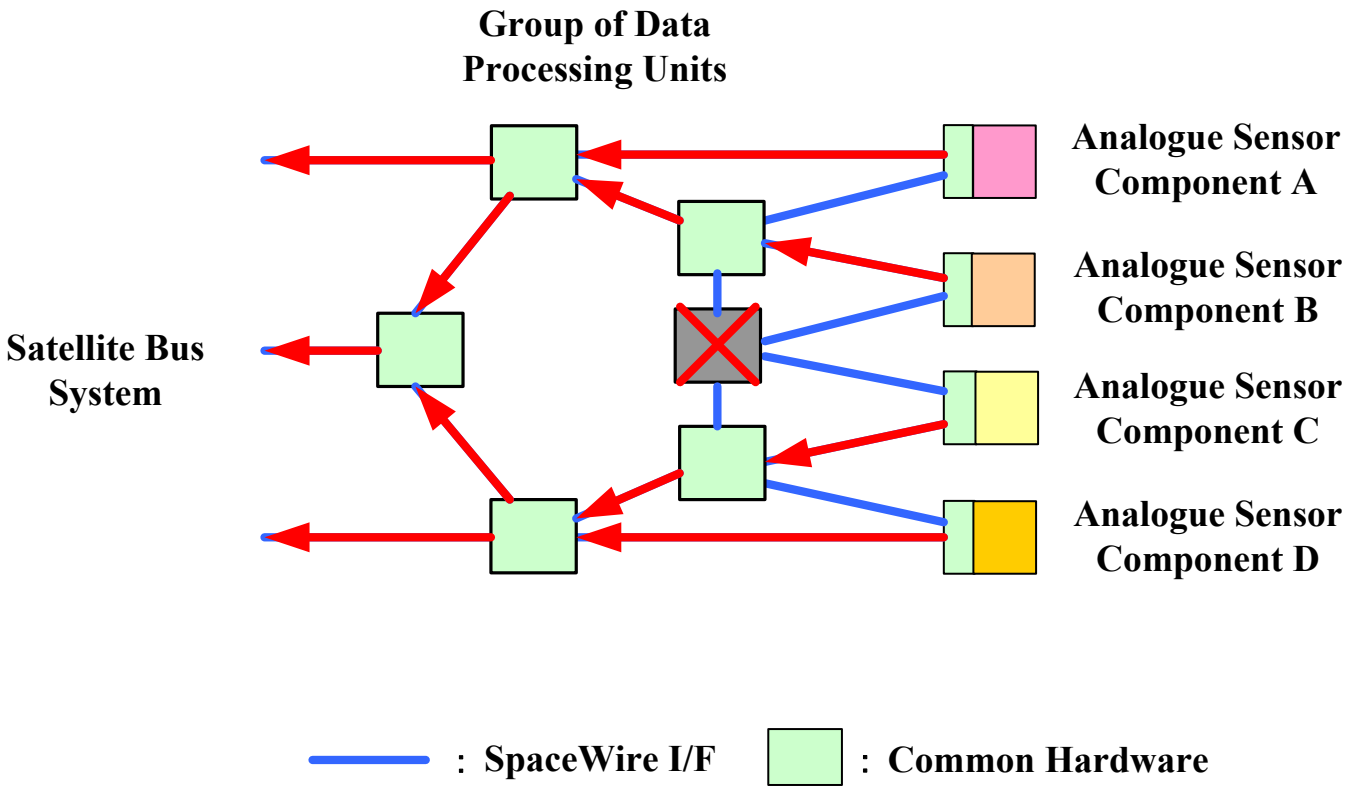
An example of fault-tolerance



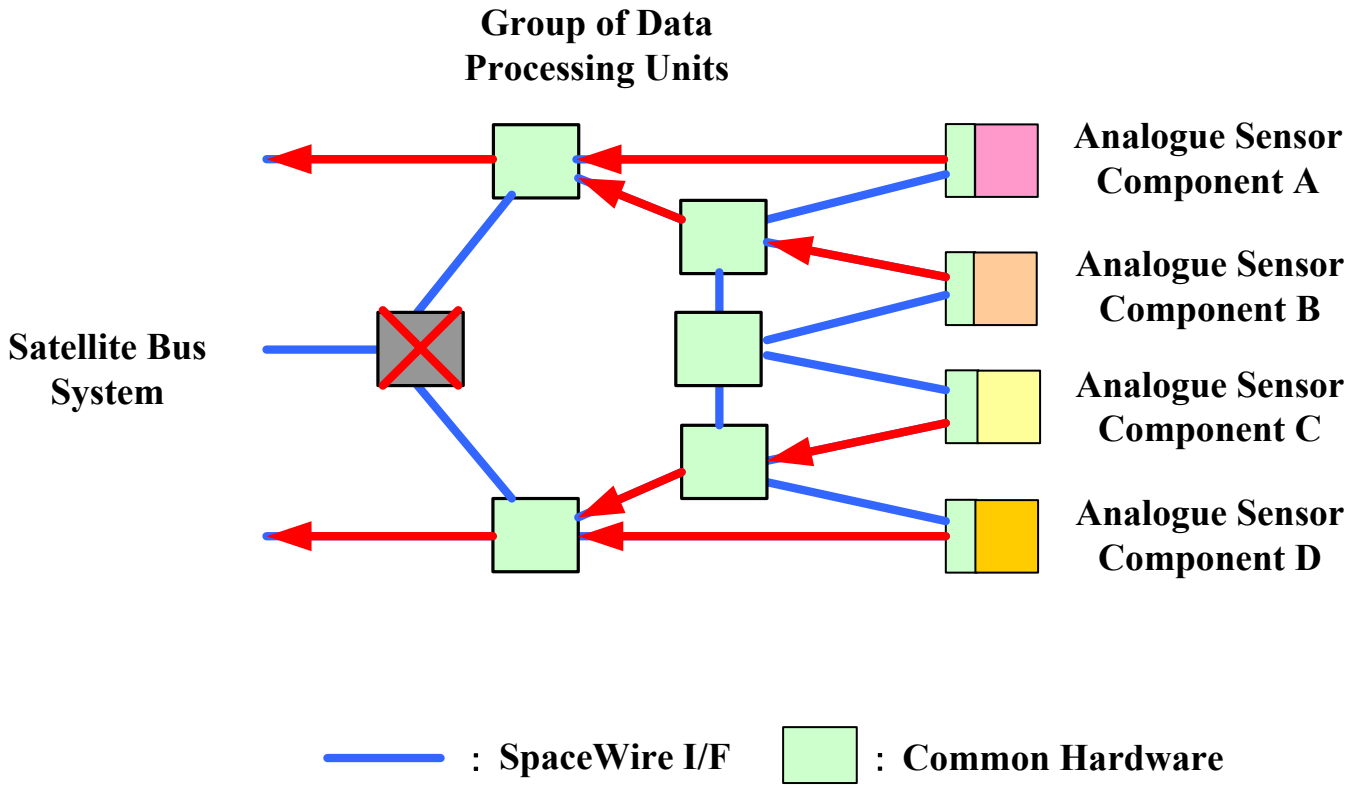
An example of fault-tolerance



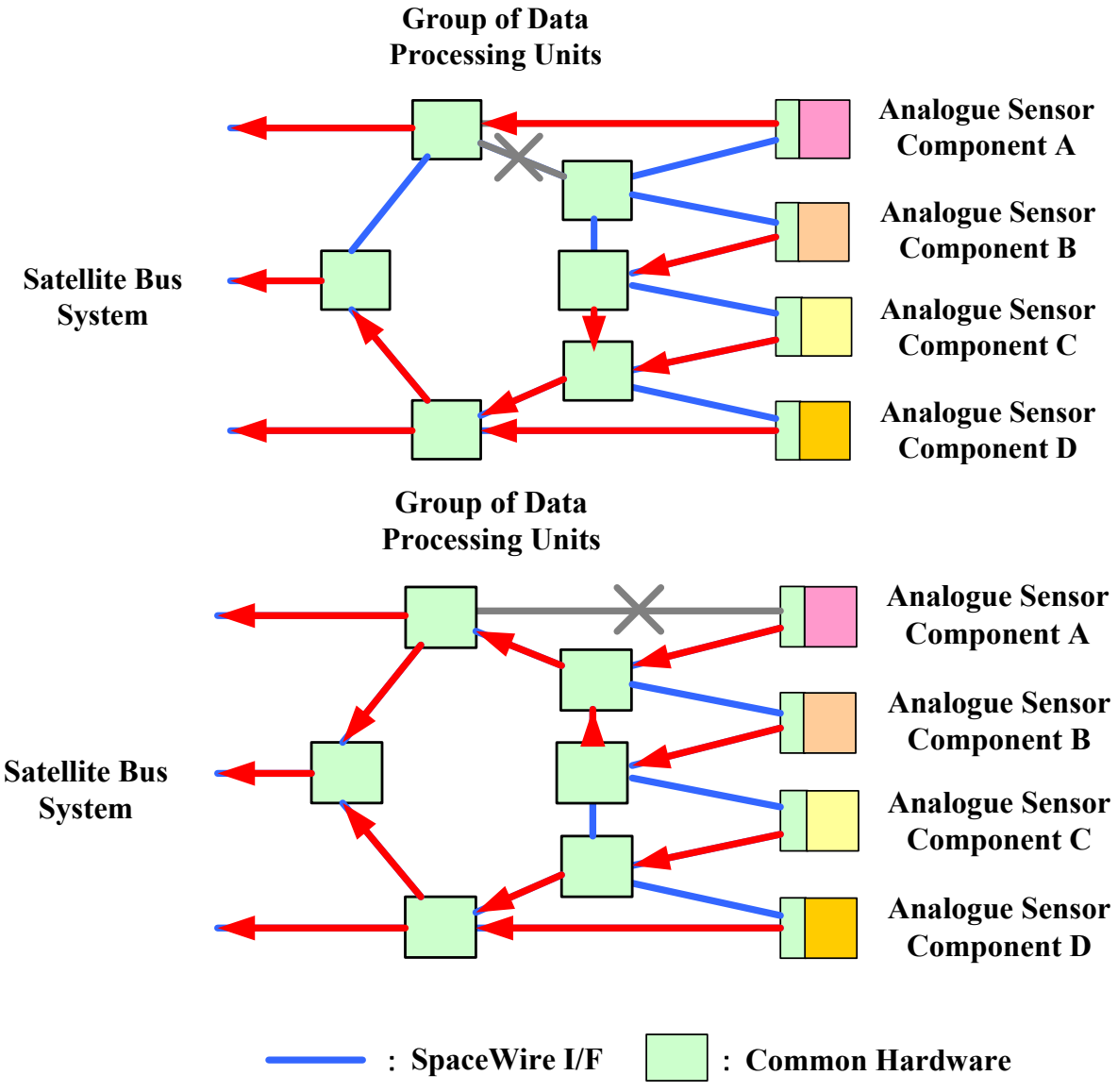
An example of fault-tolerance

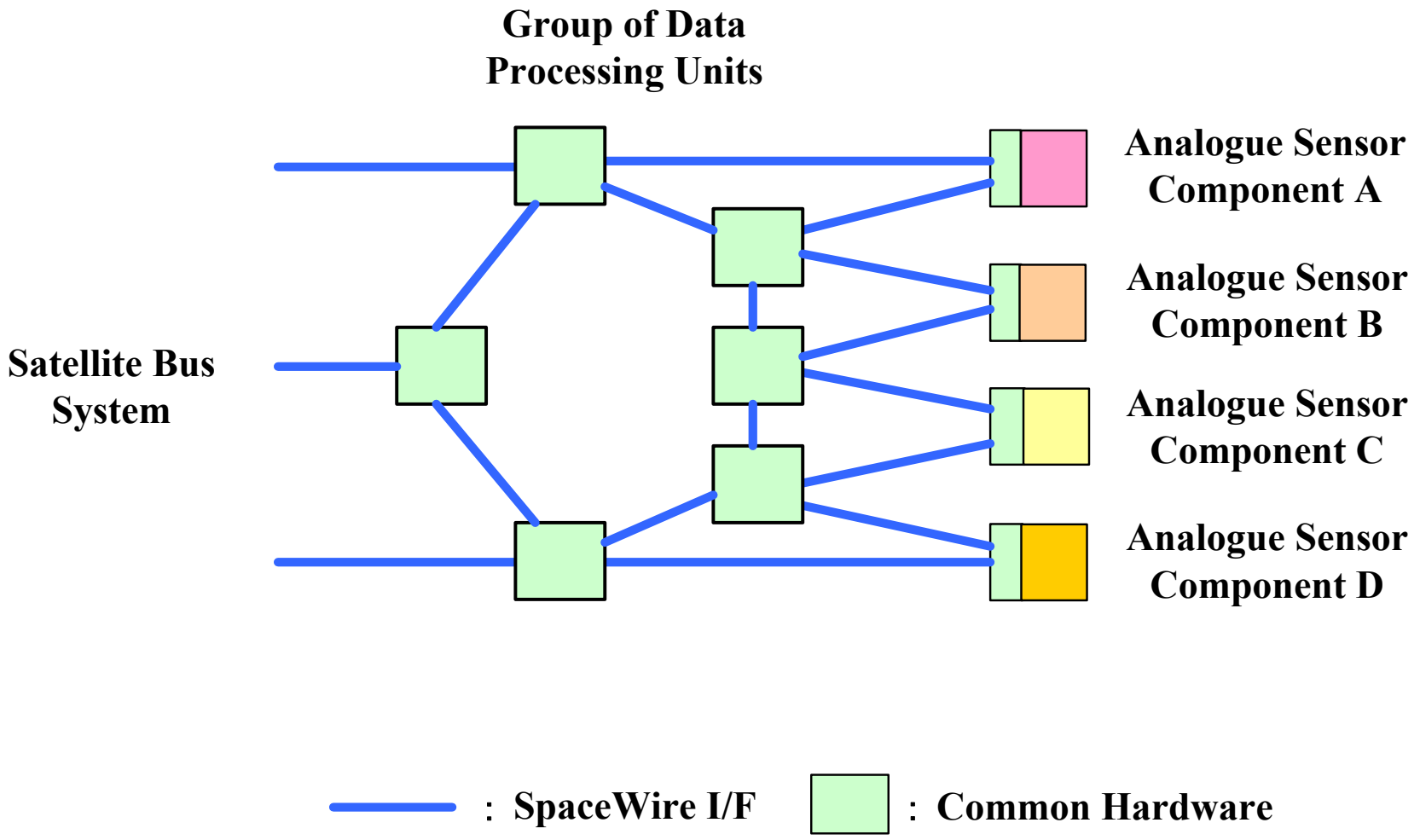


An example of fault-tolerance



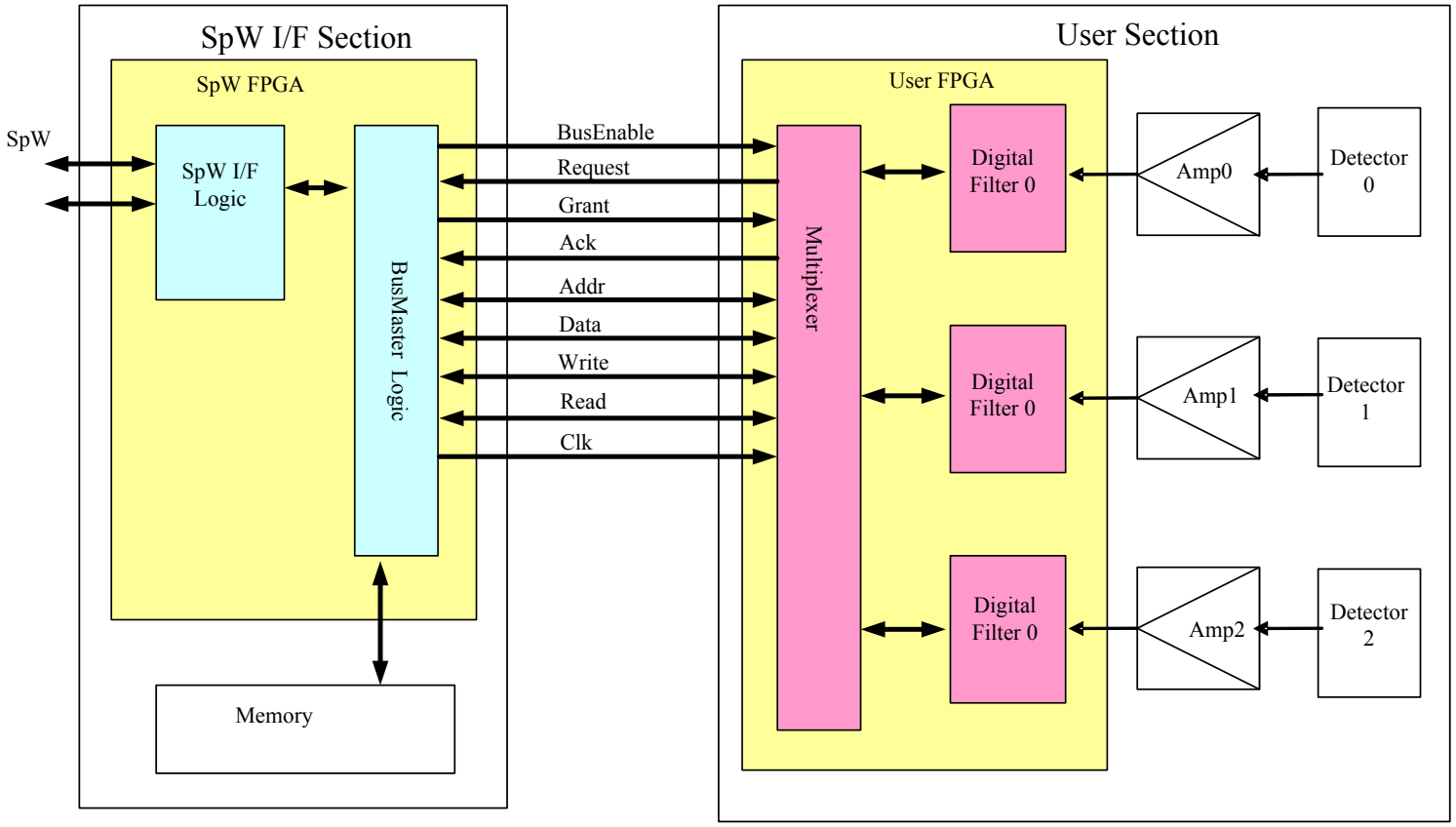
An example of fault-tolerance




Group of Data
Processing Units
Satellite Bus
System
Analogue Sensor
Component A
Analogue Sensor
Component B
Analogue Sensor
Component C
Analogue Sensor
Component D
: SpaceWire I/F
: Common Hardware

Construction of analogue sensor component

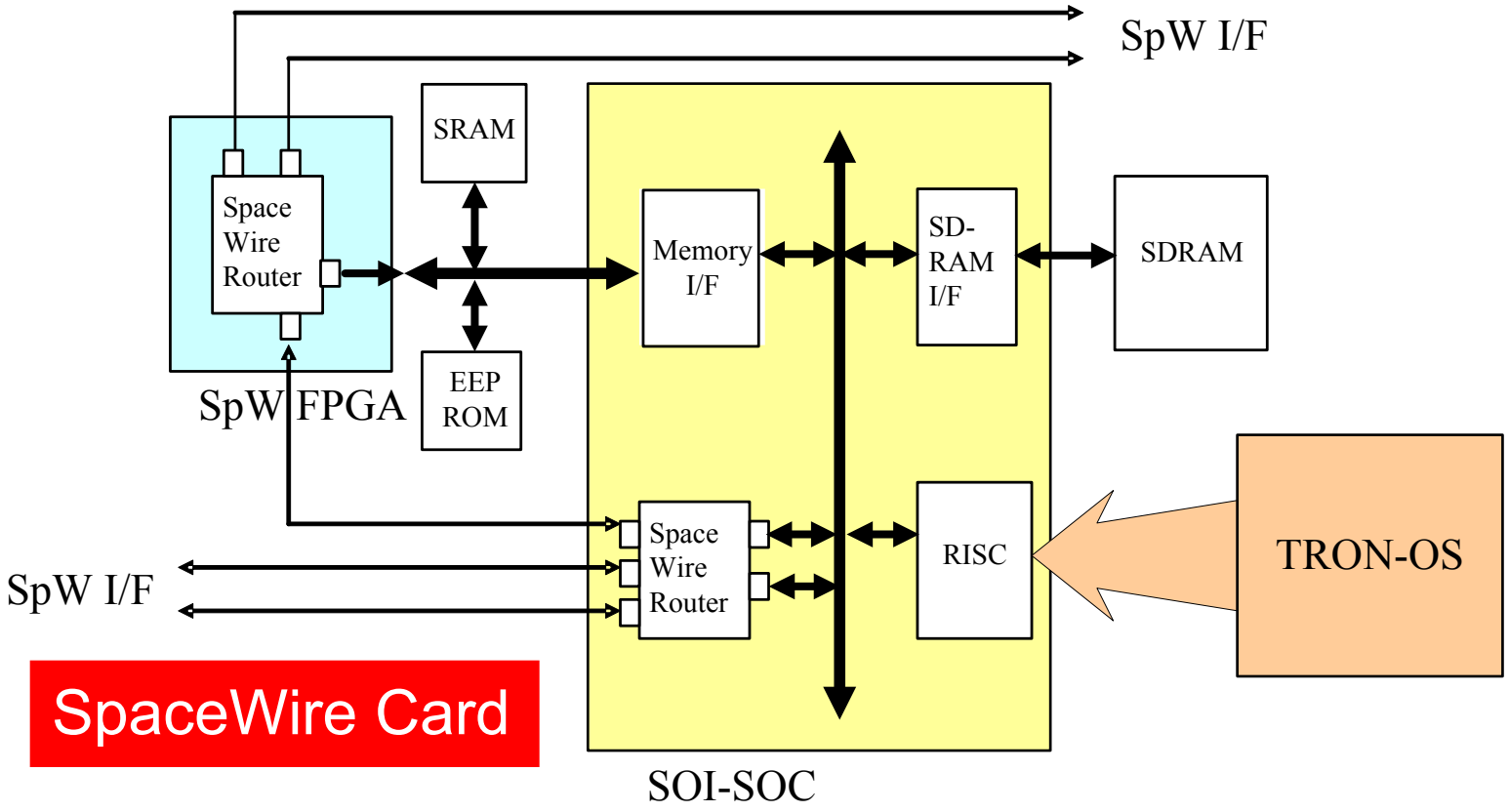
SpW I/F section and user section



To handle many component,

We introduce SpW based standard component

- SpaceWire Card -



Based on MHI's leading edge SOI technology

SOI-SOC (Silicon on Insulator – System on Chip)

New!!

-Processor

- 32 bit RISC Processor, 100MIPS
- FPU
- Cache (Icache = 16kB, Ocache = 16kB)
- MMU

-External Interface

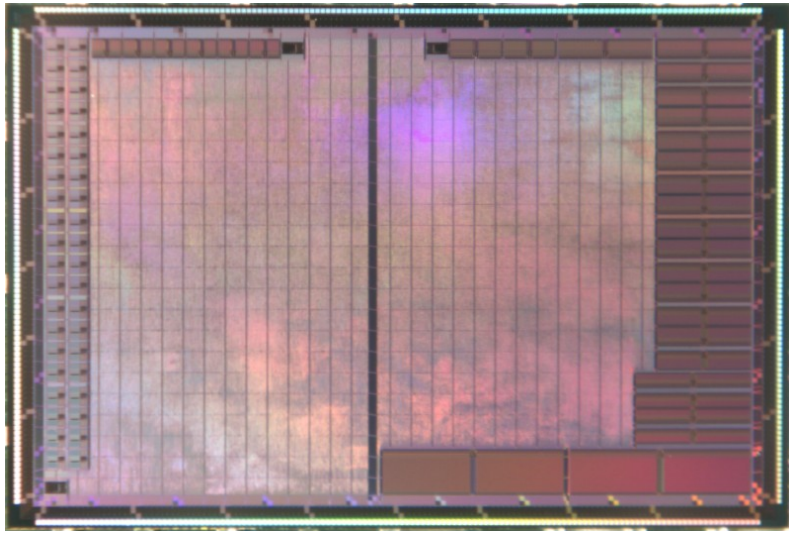
- **SpW I/F = 3ch, Routing**
- Memory I/F (SDRAM, SRAM, EEPROM, FlashROM)
- DMAC
- UART = 1ch

-Power Supply

- Core = 1.8V IO = 1.8V (3.3V)

-Radiation Characteristics

- SEU 40MeV/(mg/cm^2)
- SEL free



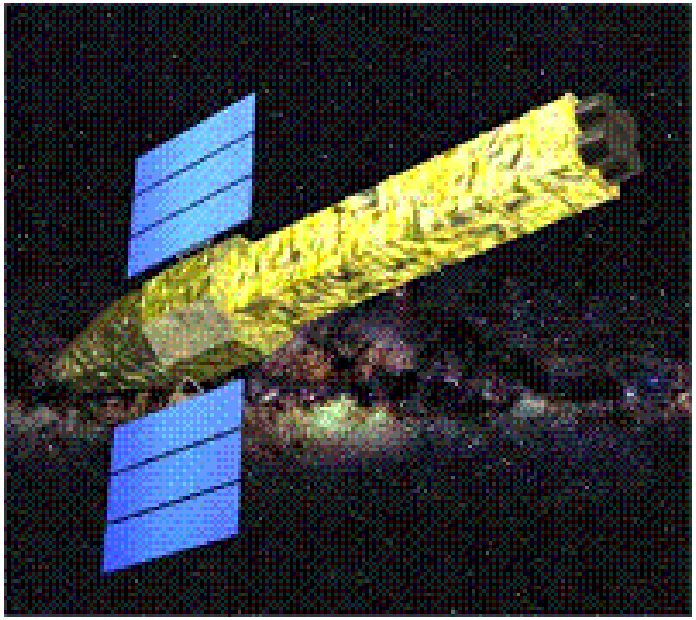
Visit our Booth to See This Chip

Summary

SpW I/F for all communication line
Common hardware and software
Connect components to form a ring

↓

To shorten development period
To reduce cost, human resource and risk
To get redundancy



NeXT Satellite

This concept will be applied to the NeXT (New X-ray Telescope) Satellite, which is scheduled to be set off in 2013 by JAXA