Real-Time Signaling in SpaceWire Networks

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Towards integral interconnection infrastructure for onboard systems

Modern satellite and spacecraft distributed on-board systems have several (3-5) separate interconnections for different types of information and signals:

- *sensor buses* for data streams from sensors and instruments
- *command buses* for commands from control units to instruments and spacecraft equipment
- *telemetry busses* for telemetry data
- *data buses* for data exchange between computing modules in the course of data and signal processing
- *time synchronization buses* for on-board synchronization
- *sideband signals* for hard real-time signaling and control

Next generation modular spacecraft avionics should move towards integral interconnection infrastructure

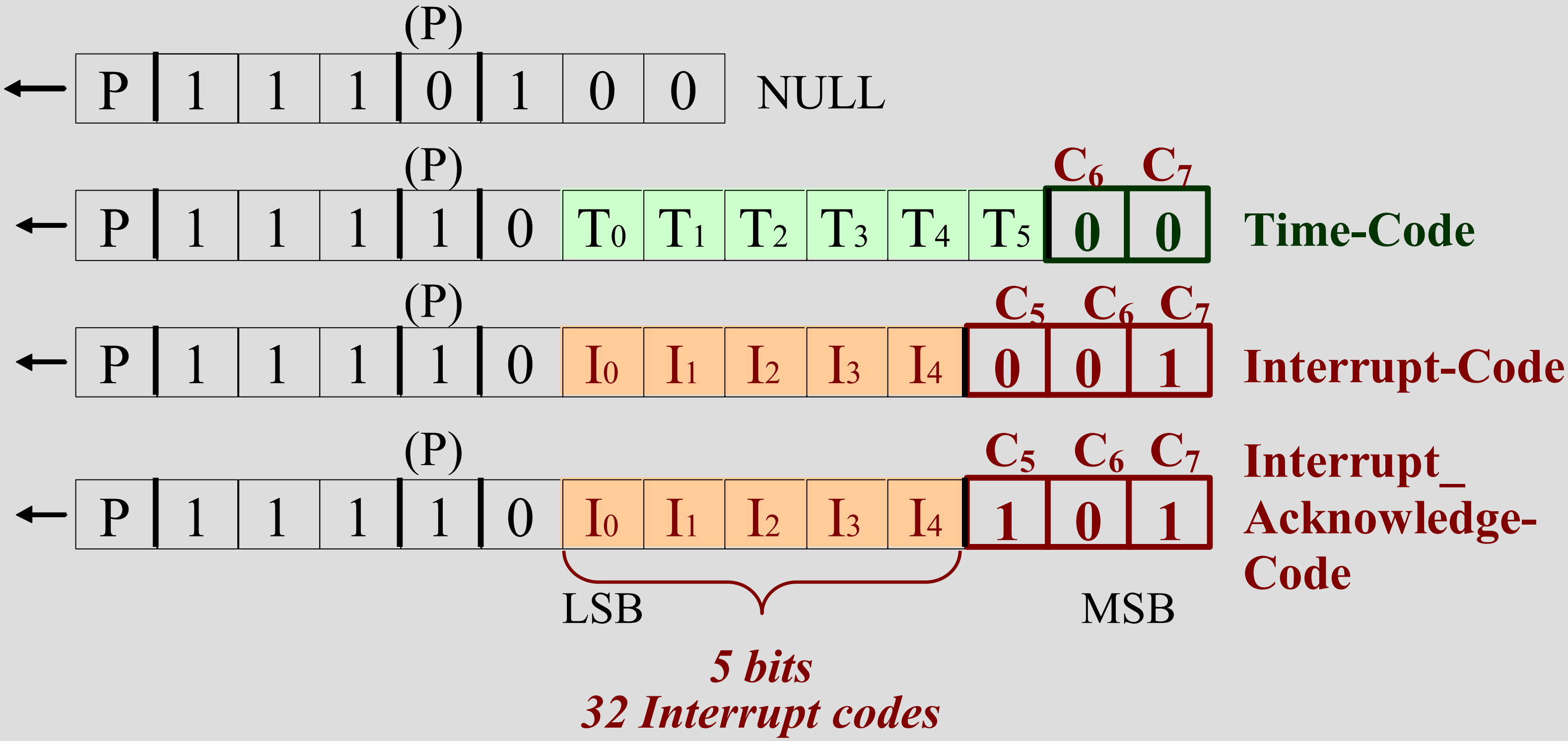
The ***SpaceWire*** is a prospective technology for integral on-board interconnections

Time codes distribution is a SpaceWire advantage

- The time codes distribution is a SpaceWire feature to substitute sideband signals for distributed systems clock synchronization. It is a clear advantage of the SpaceWire over other interconnection standards
- Other signals, besides the time codes, are needed also to be distributed in SpaceWire-based interconnections
- It is important to have them at the low protocol layer,
  in order to get high priority distribution, minimum latencies, to traverse blocked by data links, etc.
  It is ensured for time codes.
- Should be ensured for other real-time signals also.
  The SpaceWire Distributed Interrupts control codes are proposed for a SpaceWire extension

Distributed Interrupts

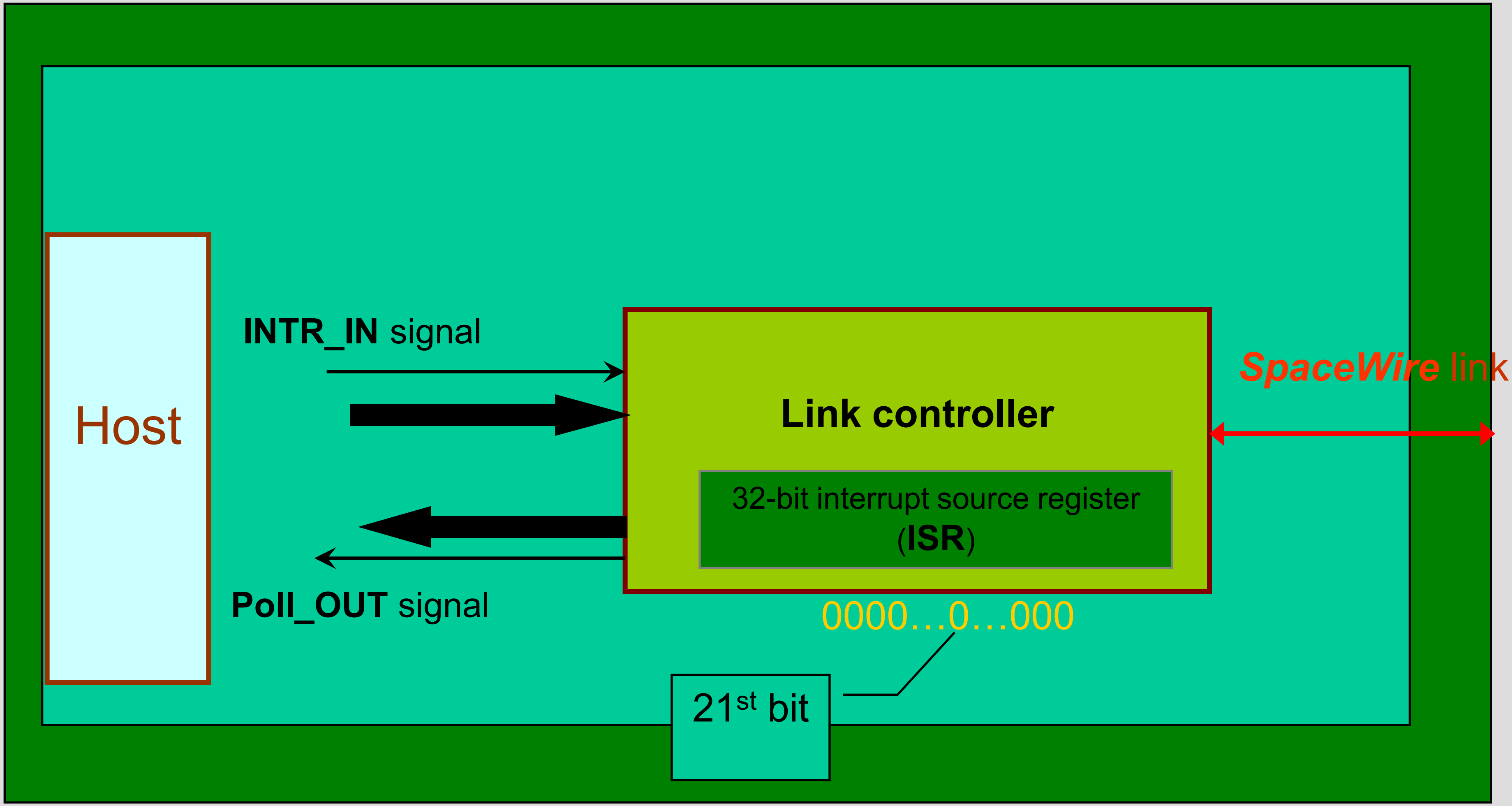
Control codes



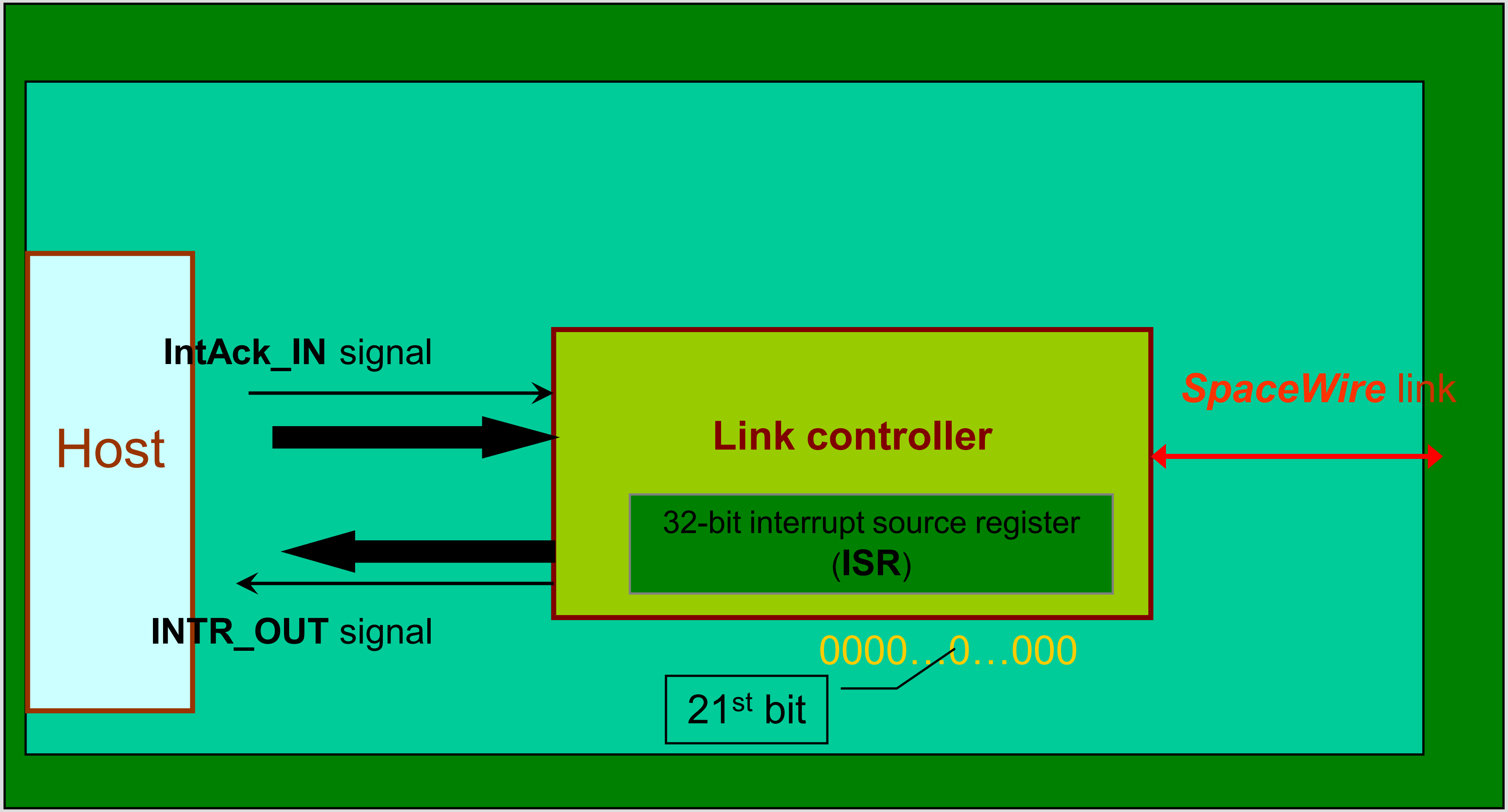
				(P)										
P	1	1	1	0	1	0	0							NULL
				(P)								C_6	C_7	
P	1	1	1	1	0	T_0	T_1	T_2	T_3	T_4	T_5	**0**	**0**	**Time-Code**
				(P)							C_5	C_6	C_7	
P	1	1	1	1	0	I_0	I_1	I_2	I_3	I_4	**0**	**0**	**1**	**Interrupt-Code**
				(P)							C_5	C_6	C_7	
P	1	1	1	1	0	I_0	I_1	I_2	I_3	I_4	**1**	**0**	**1**	**Interrupt_ Acknowledge- Code**

5 bits
32 Interrupt codes

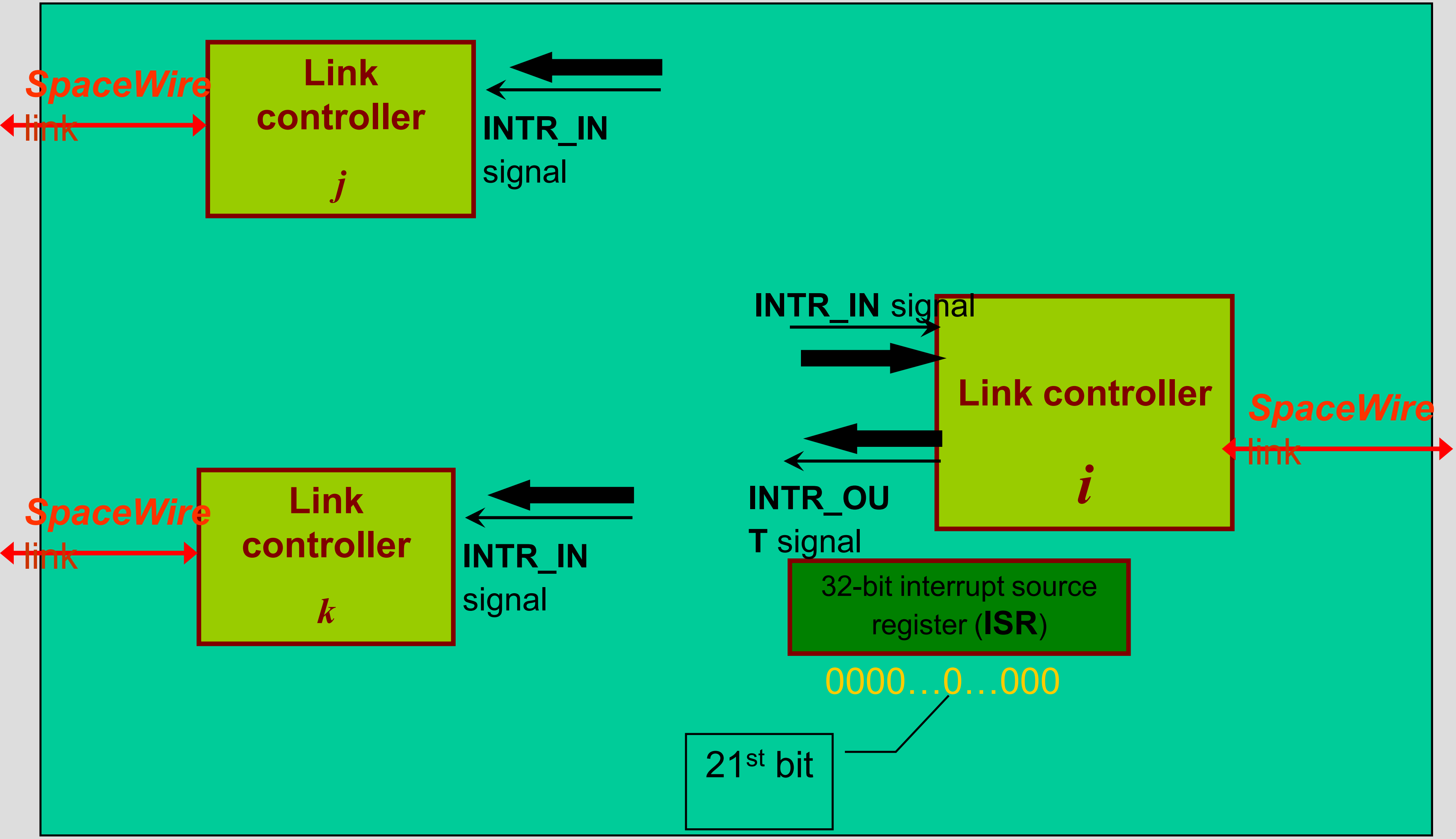
Interrupt in the *Interrupt Source* node



Interrupt code in the *Interrupt Handler* node



Interrupt code in a Router node (‘0’ in ISR)



Interrupt Codes distribution recovery in case of errors

SpaceWire network faults and errors

- Link disconnect error or parity error can cause an Int.Code/IntAck.Code loss;
- Spontaneous change of an ISR bit state as a result of intermittent faults in a node or in a router.

Interrupt mechanism is made to be tolerant:

- Networks with redundant links and circular connections (e.g. mesh, torus, fat tree) are tolerant to an Int.Code/IntAck.Code loss
- A timer per ISR bit is included in a node and in a router

ISR watchdog timers

- A timer starts at the receipt of an Interrupt-Code
- A timer resets at receipt of an Interrupt_Acknowledge-Code
- In case of timeout ***Ti*** before the timer is reset, the ISR timeout event arises
- The correspondent ISR bit ***i*** is reset to '**0**'.
- In the *Interrupt Source* link, the link also sends an Interrupt_Acknowledge-Code with the five-bit interrupt source identifier ***i***.

The ISR reset timeouts recover Interrupt –Codes distribution for following interrupt requests,
both after Interrupt–Code and IntAck-Code losses

SpaceWire real-time signalling timeout and latency characteristics.

Depend on: link bit rates, router architecture, topology of the network interconnection, control codes flow rates.

$\boldsymbol{T_{bit}}$ – one bit transfer time;
(depends on link rates)

$\boldsymbol{T_{D}}$ - worst propagation time in the network with diameter ***D***
(depends upon the SpaceWire network interconnection topology ; depends upon implementation);

$\boldsymbol{T_{wtc}}$ – Time-code transport through the router delay
(ignoring interference with previous characters/codes; depends upon implementation);

$\boldsymbol{T_{H}}$ – delay in the Interrupt Handler node
(depends upon implementation).

Timeouts

Source link the reset timeout $\boldsymbol{Ti} = \boldsymbol{T_1}$ shall be

$$T_1 > 2 * T_D + T_H$$

$$T_H > 2 * T_D$$

Reset timeout for routers and non-Interrupt-Source nodes

$\boldsymbol{Ti}=\boldsymbol{T_2}$, where $\boldsymbol{T_2} \geq \boldsymbol{T_1}$.

Time-code distribution latency

Time-code has highest priority among control codes

- Maximum time-code delivery delay:

$$\boldsymbol{T_{Tmax}} = (\boldsymbol{T_{wtc}} + 13\ \boldsymbol{T_{bit}})*(\boldsymbol{D}-1) + (14\ \boldsymbol{T_{bit}})*\boldsymbol{D}$$

$$= \boldsymbol{T_{wtc}\ (D\text{-}1) + T_{bit}\ (27\ D - 13).}$$

For $\boldsymbol{D}$=5, $\boldsymbol{T_{wtc}}$ = 200 ns

it will give $\boldsymbol{T_{Tmax}} = \mathbf{1{,}1\ \mu s}$.

Interrupt codes distribution latency

- Several Interrupt codes (up to 32) can run concurrently in the network, may come (theoretically) simultaneously to a router.
- They will have to let pass ahead a Time-code that can also appear at the moment.

The maximum Interrupt-code delivery delay, pessimistic:

$$T_{Imax} = (D\text{-}1)\ {*}(T_{wtc} + 13T_{bit} + 14T_{bit} + 31{*}14{*}T_{bit}) + (14T_{bit}){*}D$$

$$= (D\text{-}1){*}(T_{wtc} + 461 T_{bit}) + 14T_{bit}{*}\mathrm{D}.$$

For D=5, at 400 Mb/s it will gi $T_{Imax} = 5{,}6\ \mu s$.

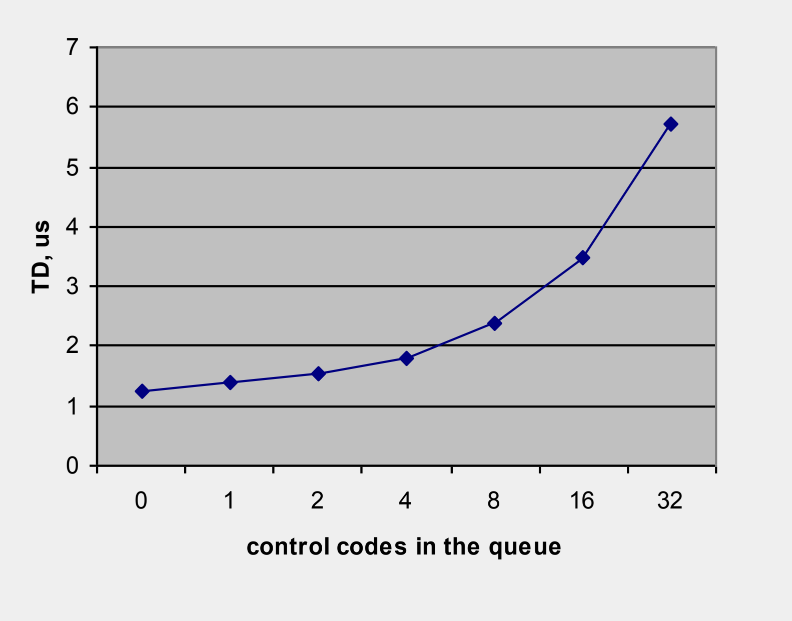
Don't be greedy when selecting link rates

Interrupt codes distribution latency (2)

More realistic estimations:

q - an average number of waiting control codes in a router at the moment of the Interrupt code arrival.

$$T_D = (D-1)*(T_{wtc} + 27T_{bit} + 14\, q*T_{bit}) + (14T_{bit})*D$$



For D=5, at 400 Mb/s; for q < 6, $T_D < 2\mu s$.

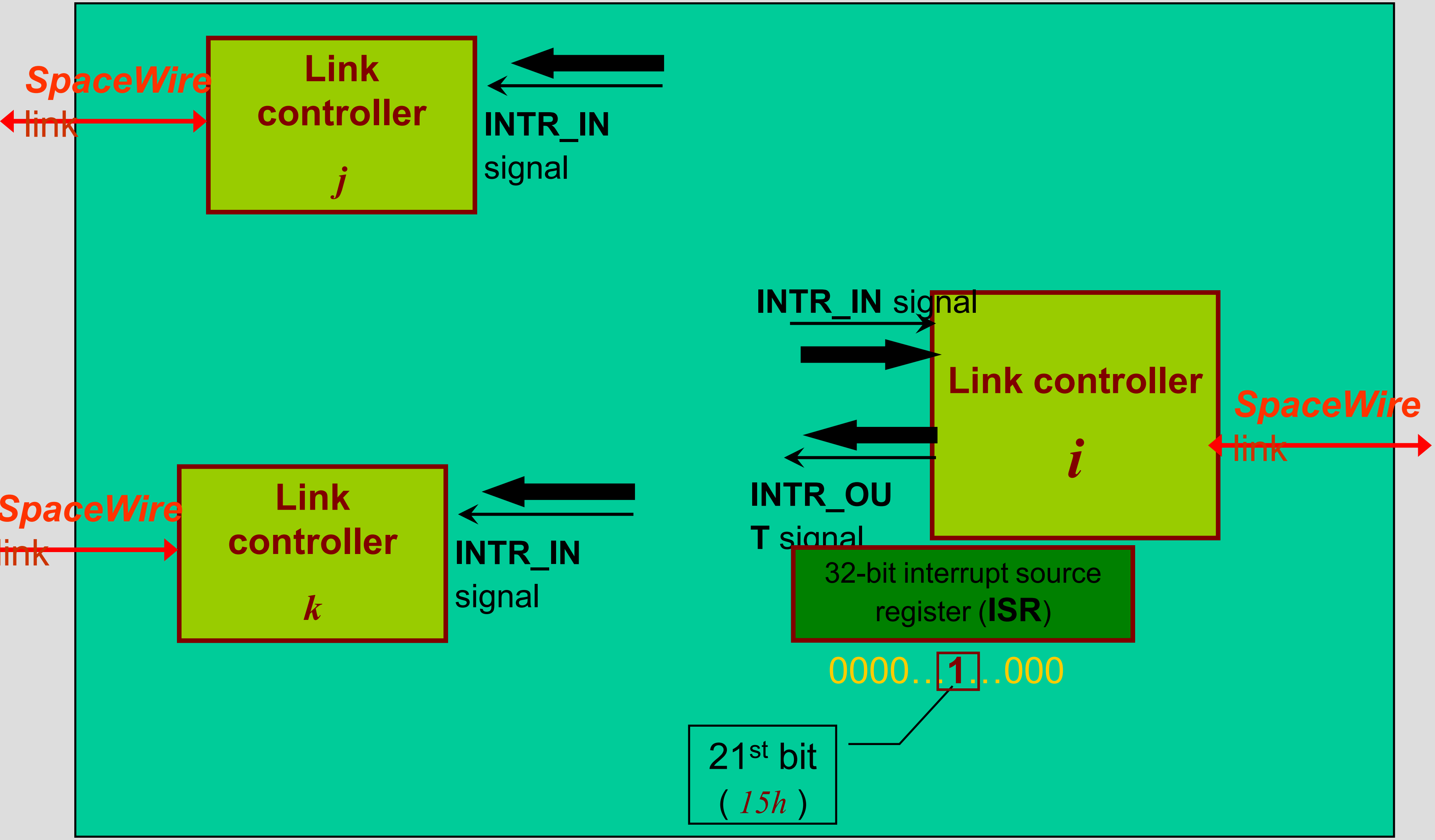
Conclusion

- Former sideband signals, like interrupts, are integrated into SpaceWire interconnections
- Up to 32 different signals can be distributed in an interconnection simultaneously
- Interrupt/IntAck codes are specified at the Symbol level.
  They have high priority for transmission and switching
  (next to Time codes)
- Interrupt/IntAck codes are distributed regardless of data transmission, cutting into data symbols flow at any link – idle, busy, blocked for data
- Interrupt/IntAck codes ensure low latency distribution, a couple of microseconds, that is appropriate for most practical cases.
- Implemented in “MultiFlight“ SpaceWire ASIC chips and in our FPGA-based SpaceWire link controllers IP, bridges and routers

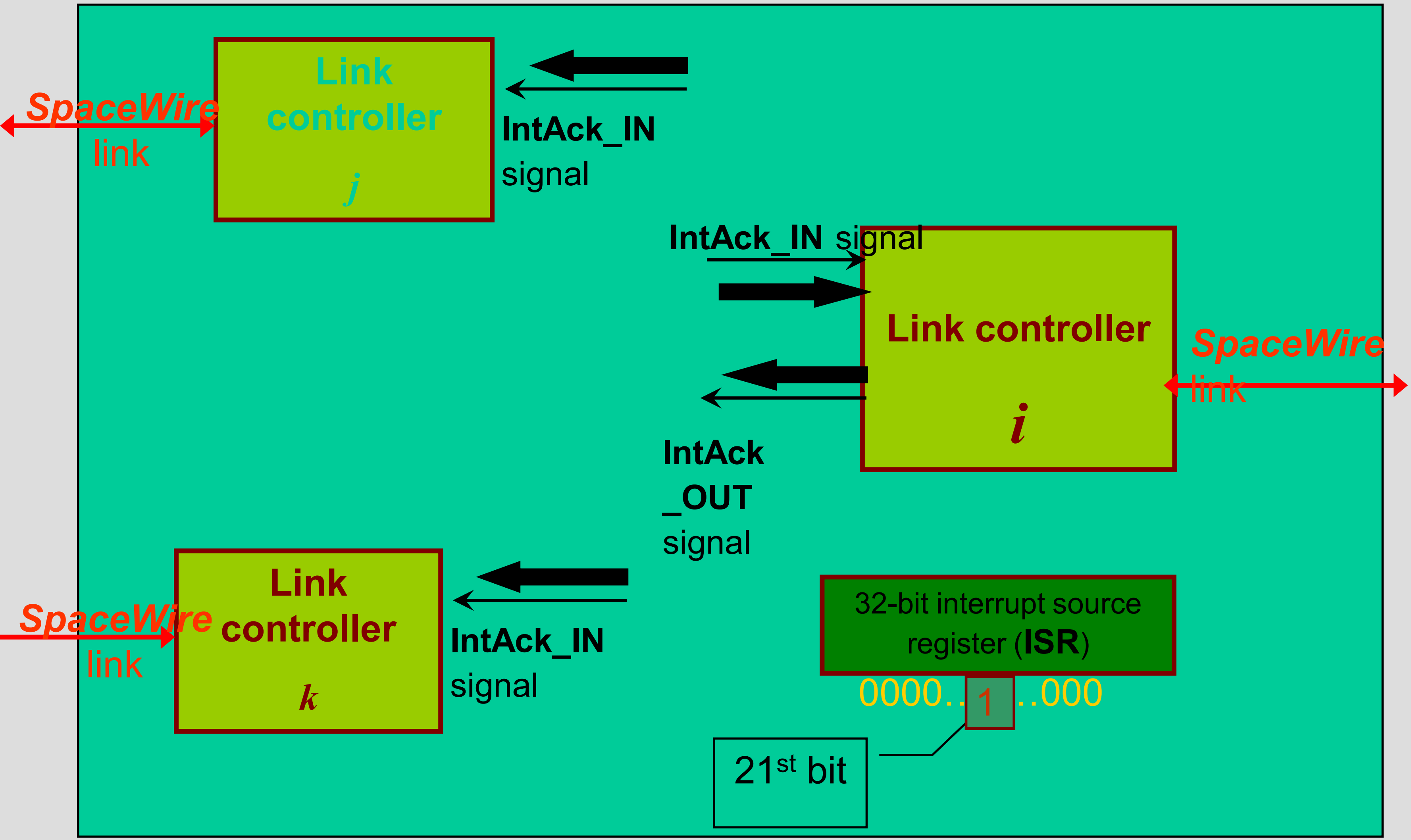
Thank you!

Back up

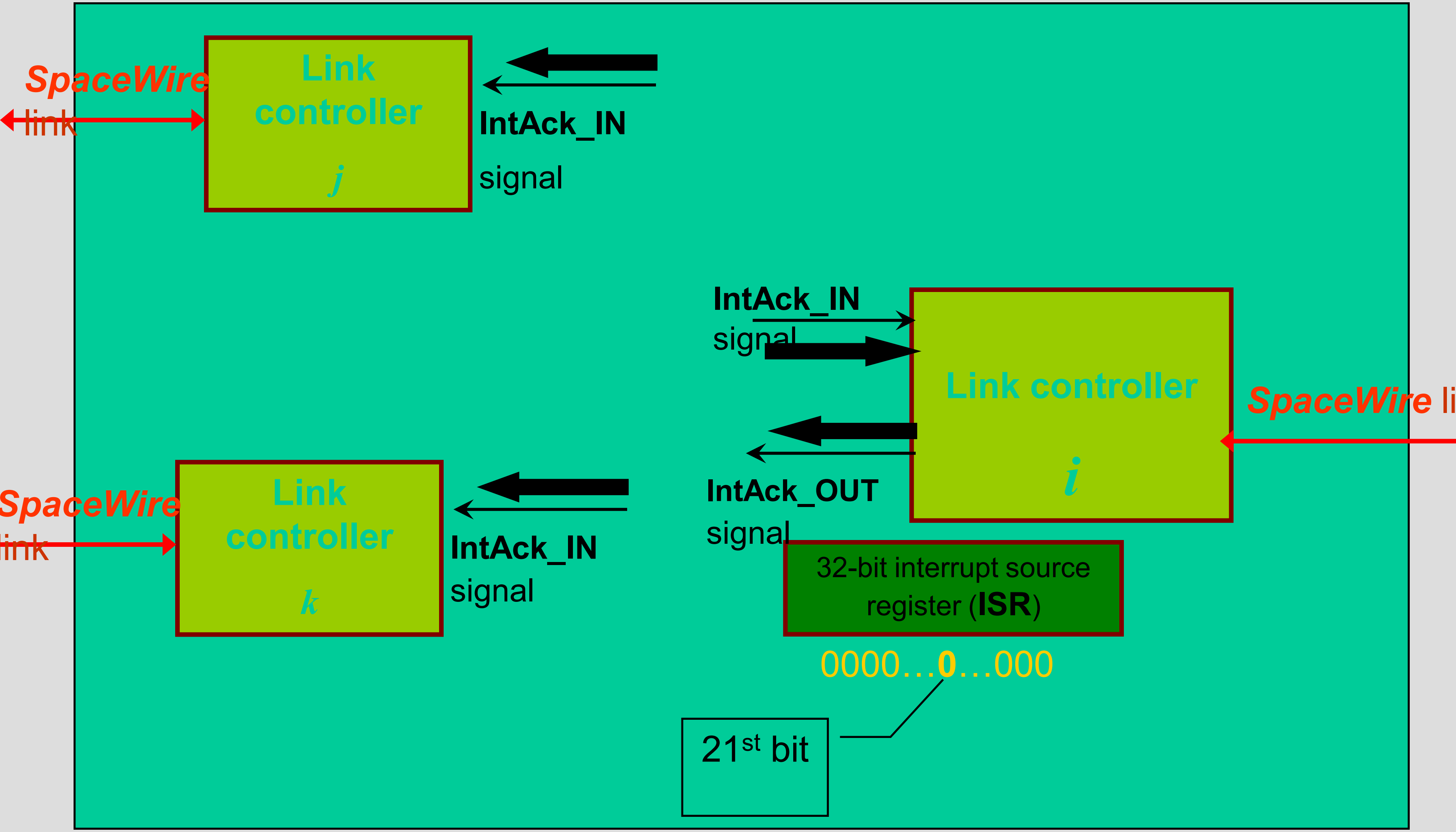
Interrupt code processing in a Router node ('1' in ISR)

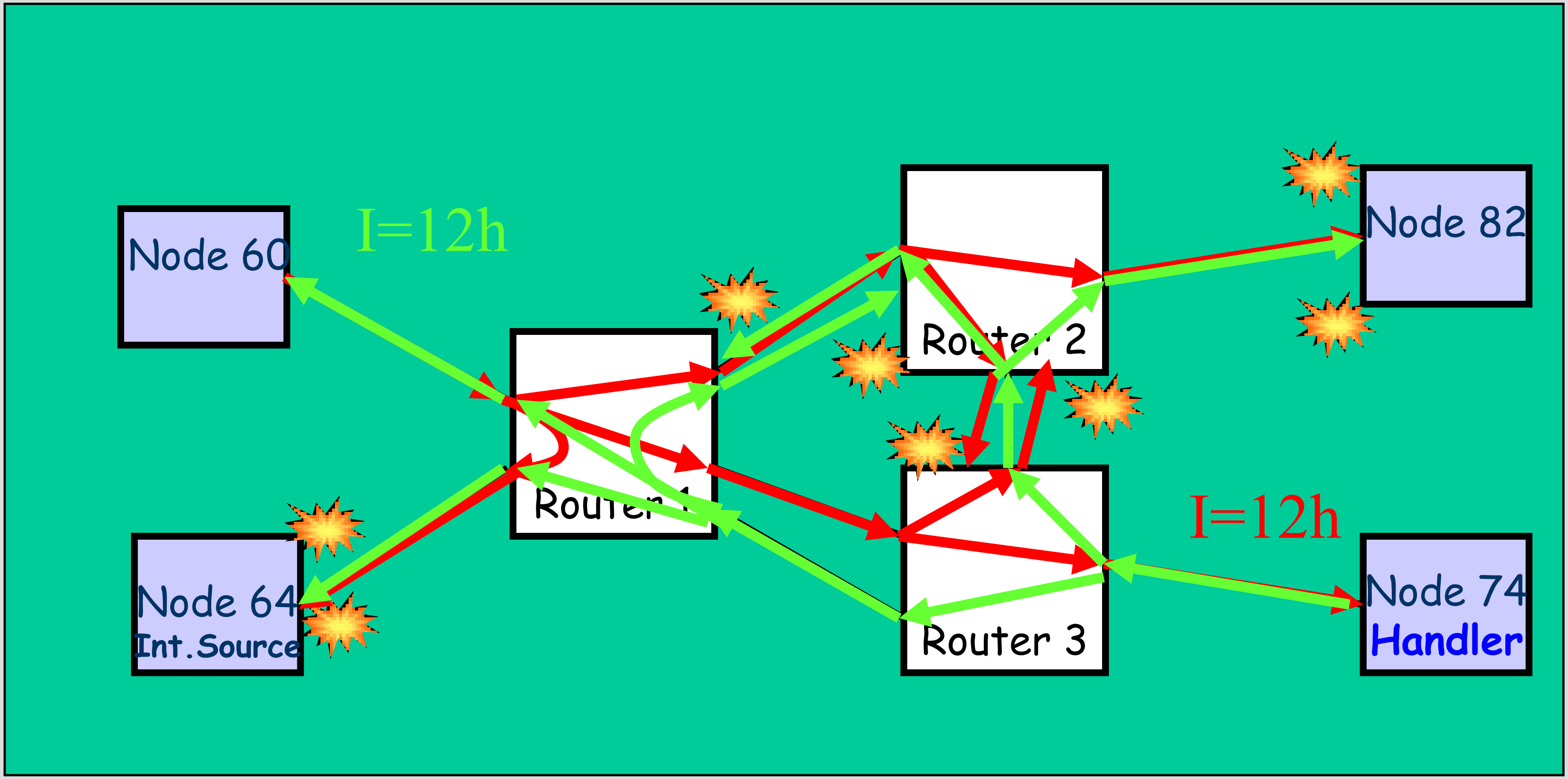


Interrupt_Acknowledge code processing in a Router node ('1' in ISR)



Interrupt_Acknowledge code in a Router node ('0')





→ Interrupt-code: interrupt request. IRQ vector I=12h

→ • IntAck-code: Acknowledges the interrupt accepted for processing.