RAD750™ SpaceWire Enabled Flight Computer for Lunar Reconnaissance Orbiter

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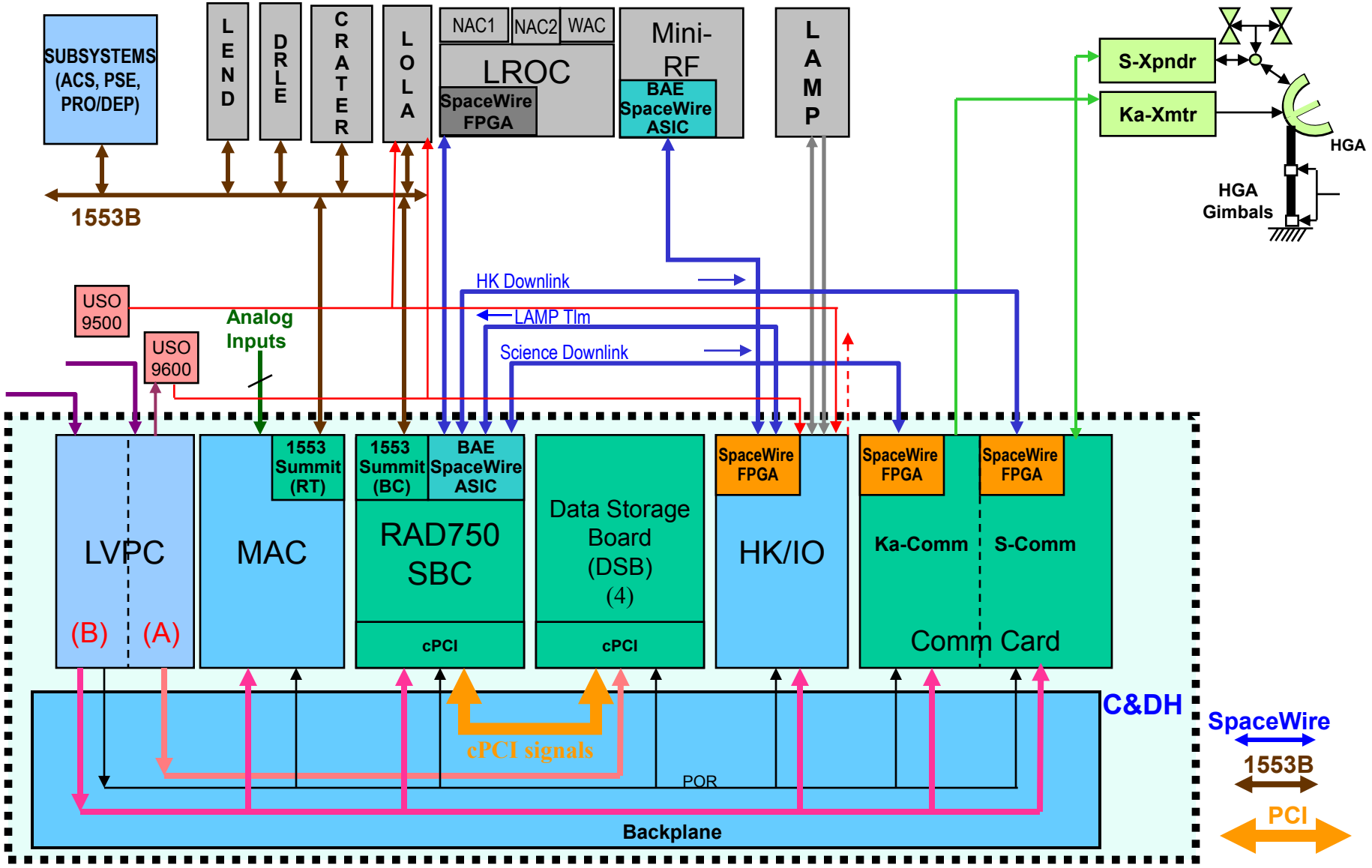
2007 International SpaceWire Conference

LRO Command and Data Handling (C&DH) / Spacecraft Architecture



RAD750 CompactPCI LRO Single Board Computer

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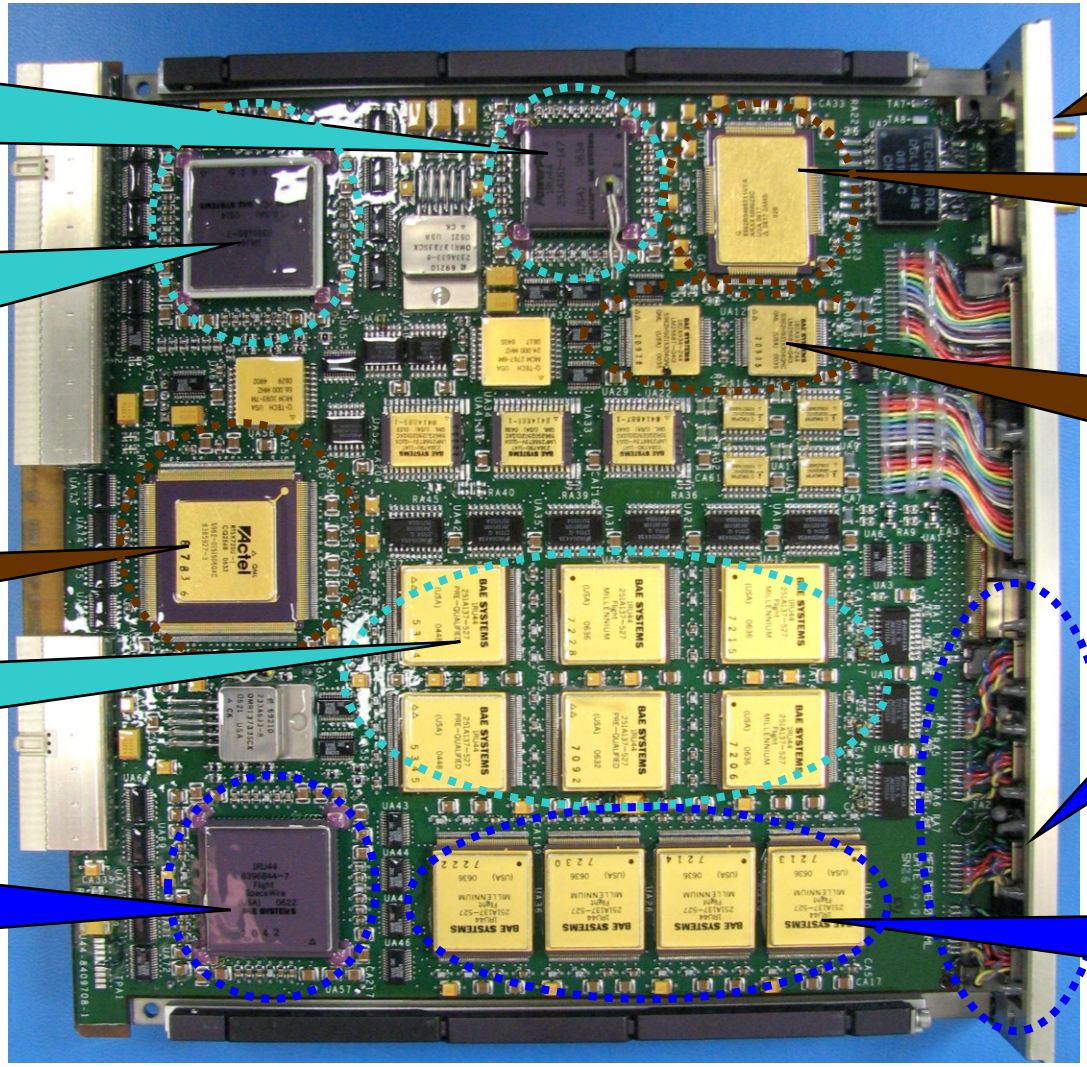


BAE Systems 132 MHz RAD750 PowerPC Microprocessor

BAE Systems Enhanced Power PCI Bridge ASIC

SPIF Actel FPGA

BAE Systems SRAM (36 MB) for processor

BAE Systems SpaceWire ASIC

MIL-STD-1553 Connectors (2)

Aeroflex SuMMIT ASIC

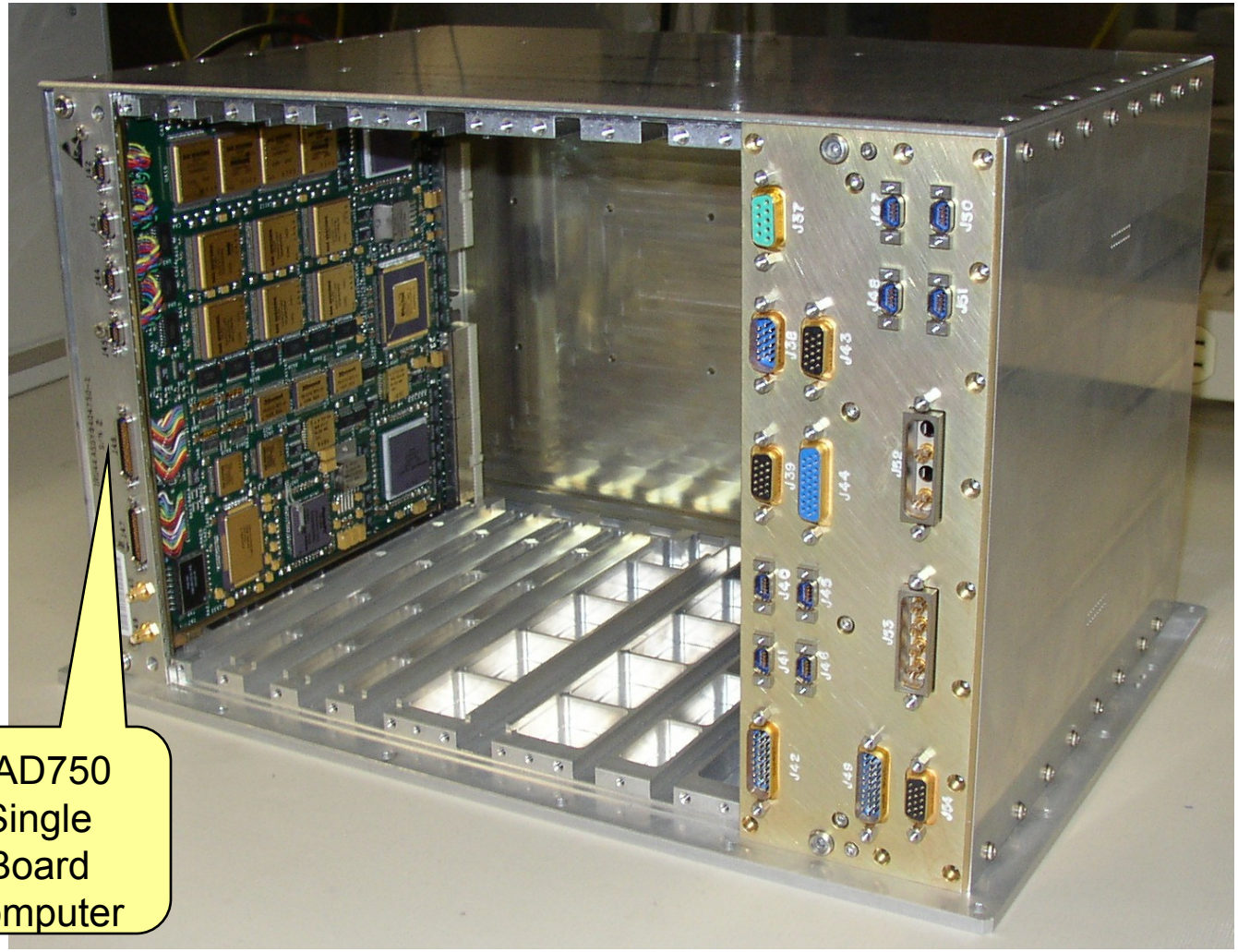
BAE Systems SRAM (64KB) for 1553

SpaceWire Connectors (4)

BAE Systems SRAM (8 MB) for SpaceWire

CompactPCI 6U-220 Board Format

RAD750 Computer In the LRO C&DH Enclosure



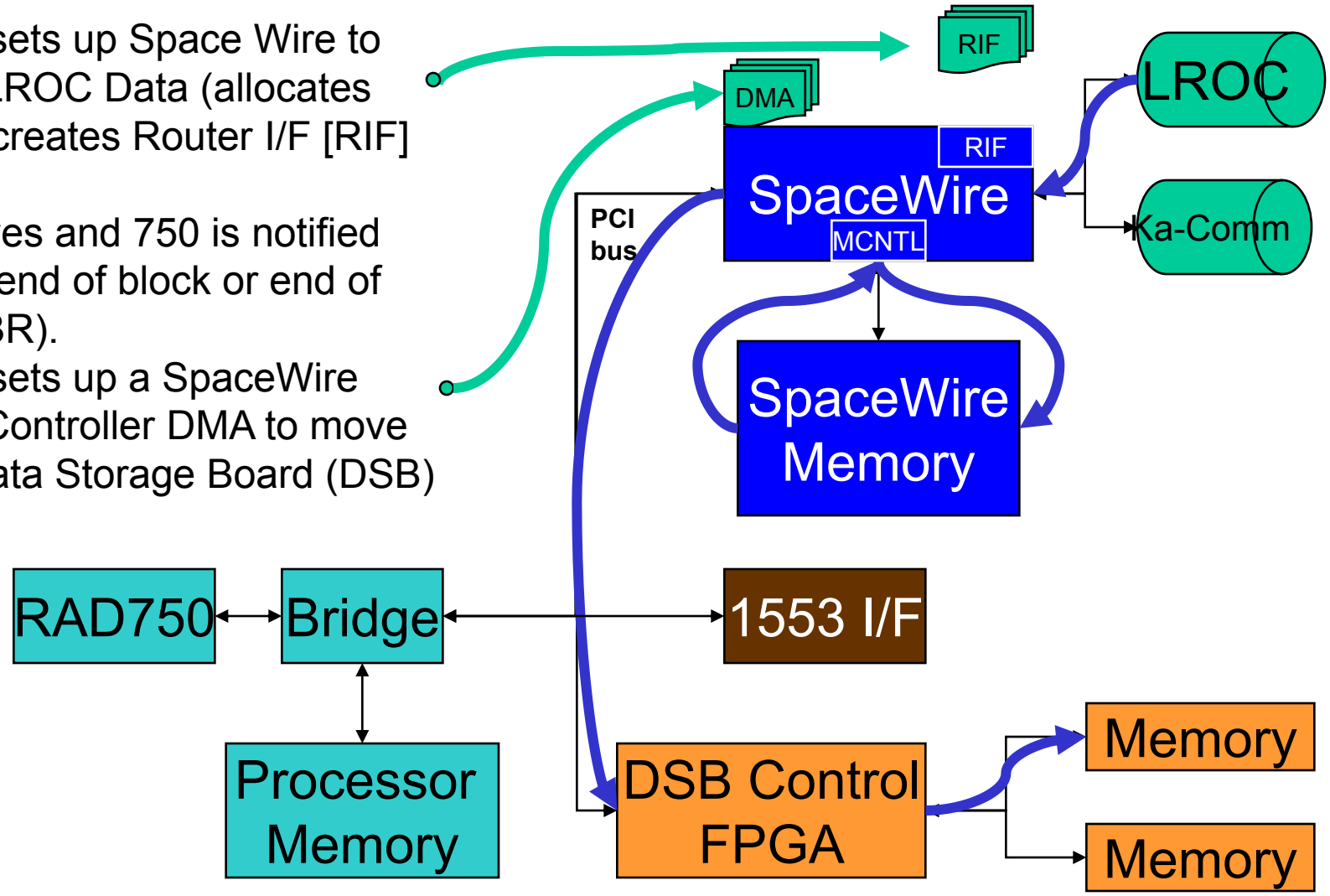
Single Board Computer Deliveries:

- Breadboards – 2006
- Engineering Units – Early 2007
- Flight Units – June 2007

C&DH Unit now inserted into LRO FlatSat testbed

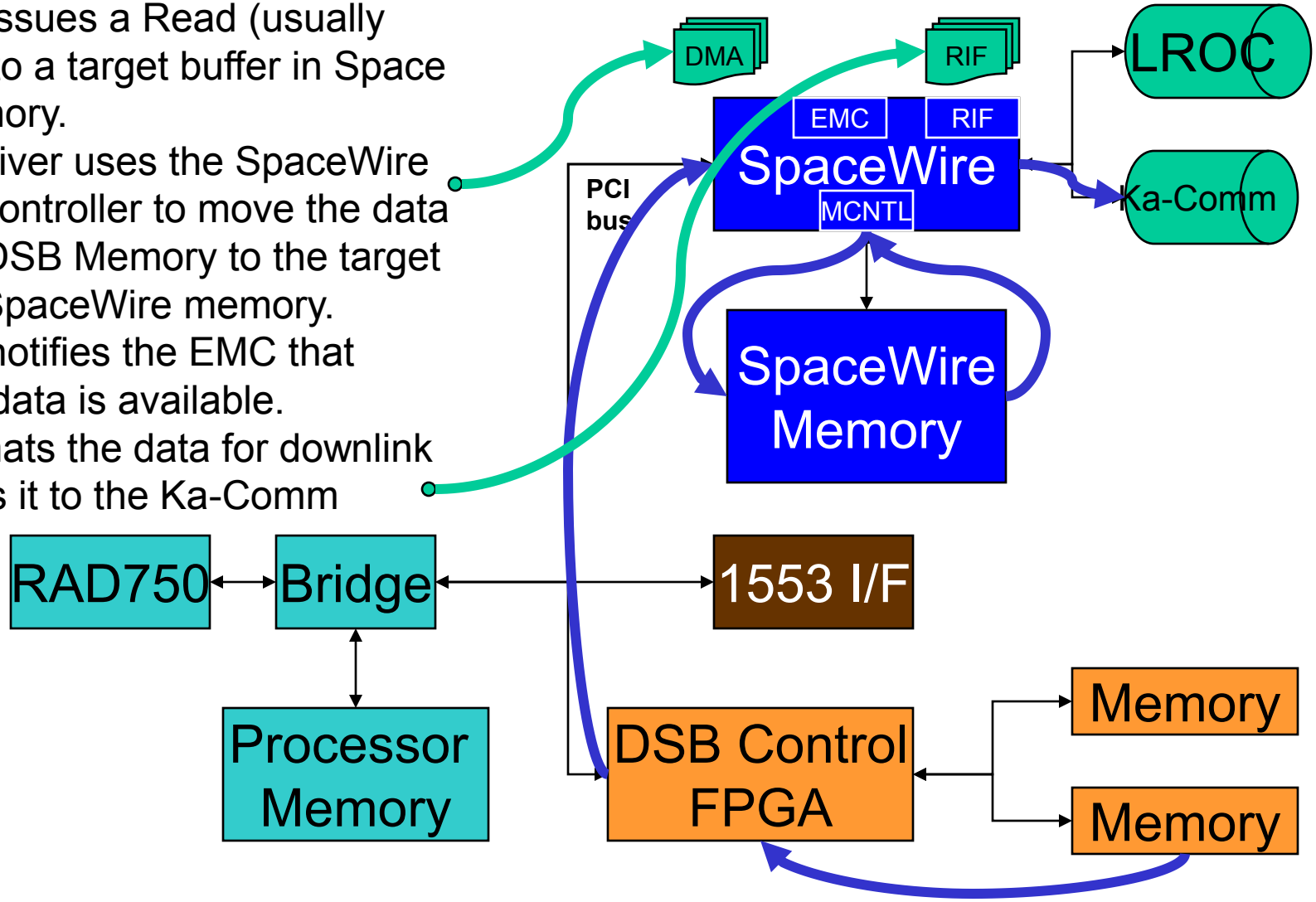
SpaceWire Data Transfer: LROC to Storage Memory

1. RAD750 sets up Space Wire to Receive LROC Data (allocates memory, creates Router I/F [RIF] DMAs).
2. Data Arrives and 750 is notified (either at end of block or end of packet TBR).
3. RAD750 sets up a SpaceWire Memory Controller DMA to move data to Data Storage Board (DSB) memory.



SpaceWire Data Transfer: Memory to Downlink

1. RAD750 issues a Read (usually 1Mbyte) to a target buffer in Space Wire Memory.
2. Device Driver uses the SpaceWire Memory controller to move the data from the DSB Memory to the target buffer in SpaceWire memory.
3. RAD750 notifies the EMC that downlink data is available.
4. EMC formats the data for downlink and sends it to the Ka-Comm



Next Generation RAD750 Single Board Computer

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