Space Cube 2
an Onboard Computer based on *Space Cube Architecture*

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SpaceWire in Japan

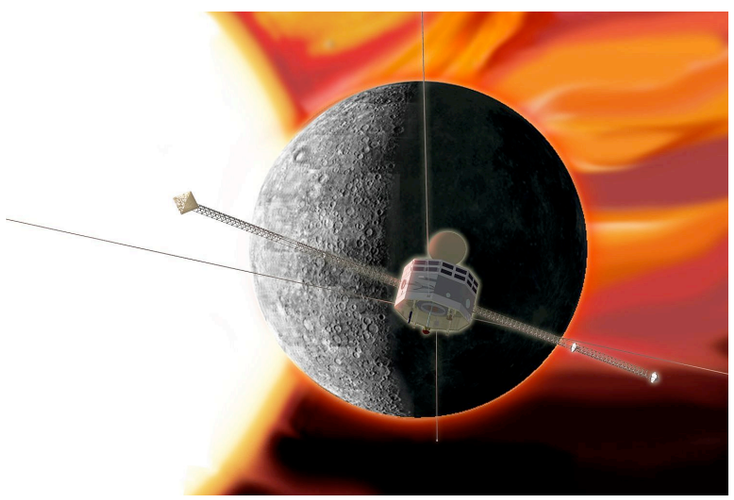
After many discussions/experiments
We have decided to choose

Space Wire

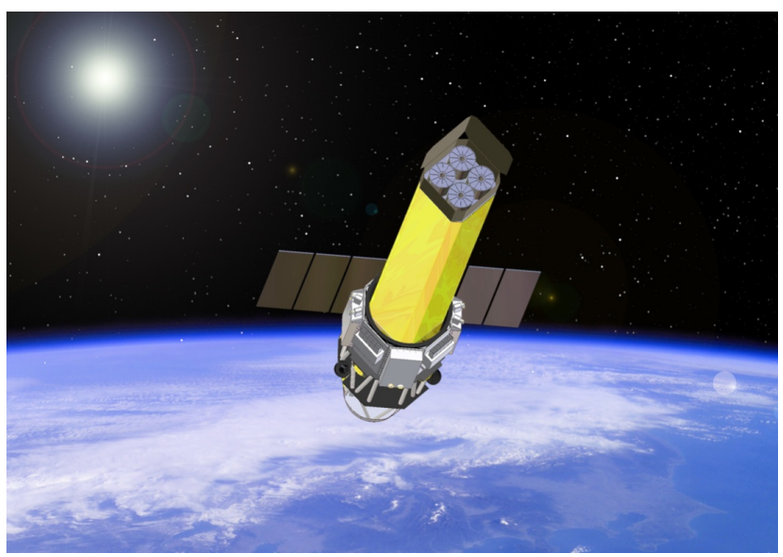
as a standard to be implemented in future scientific satellites.

Next Step is to define a standard architecture for scientific satellites, which often require different specifications of how the components are linked and controlled, depending on their scientific objectives.

Bepi Colombo / MMO (2013)



X-ray Astronomy - NeXT -(planned 2013)



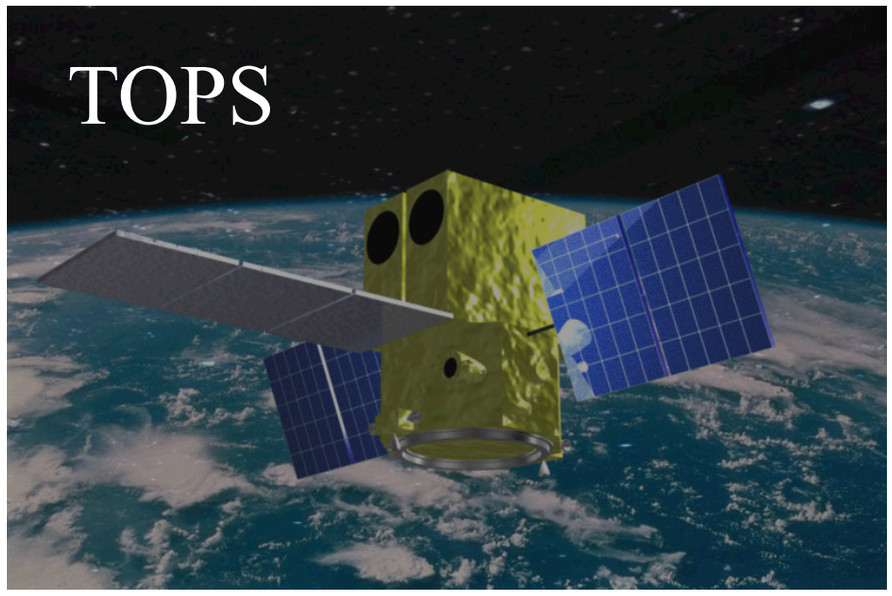
Small Science Satellite Project in Japan

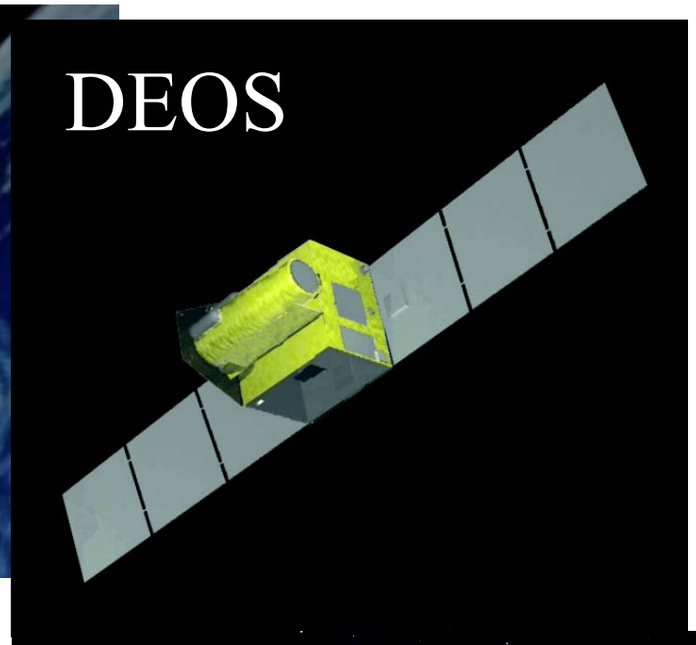
plan to launch 3 satellites in 5 years

400 kg in low earth orbit

Launch 2011

Other Candidates for 2012-2015





And More

Small science missions have to be realized as quick as possible:

How we can develop space crafts in a short time, without losing reliability, with reasonably low cost...

Modular Structure with SpW interface would be the key

The Goal

1. Modularity, Flexibility, Scalability
(Applicable to Med/Small satellites)

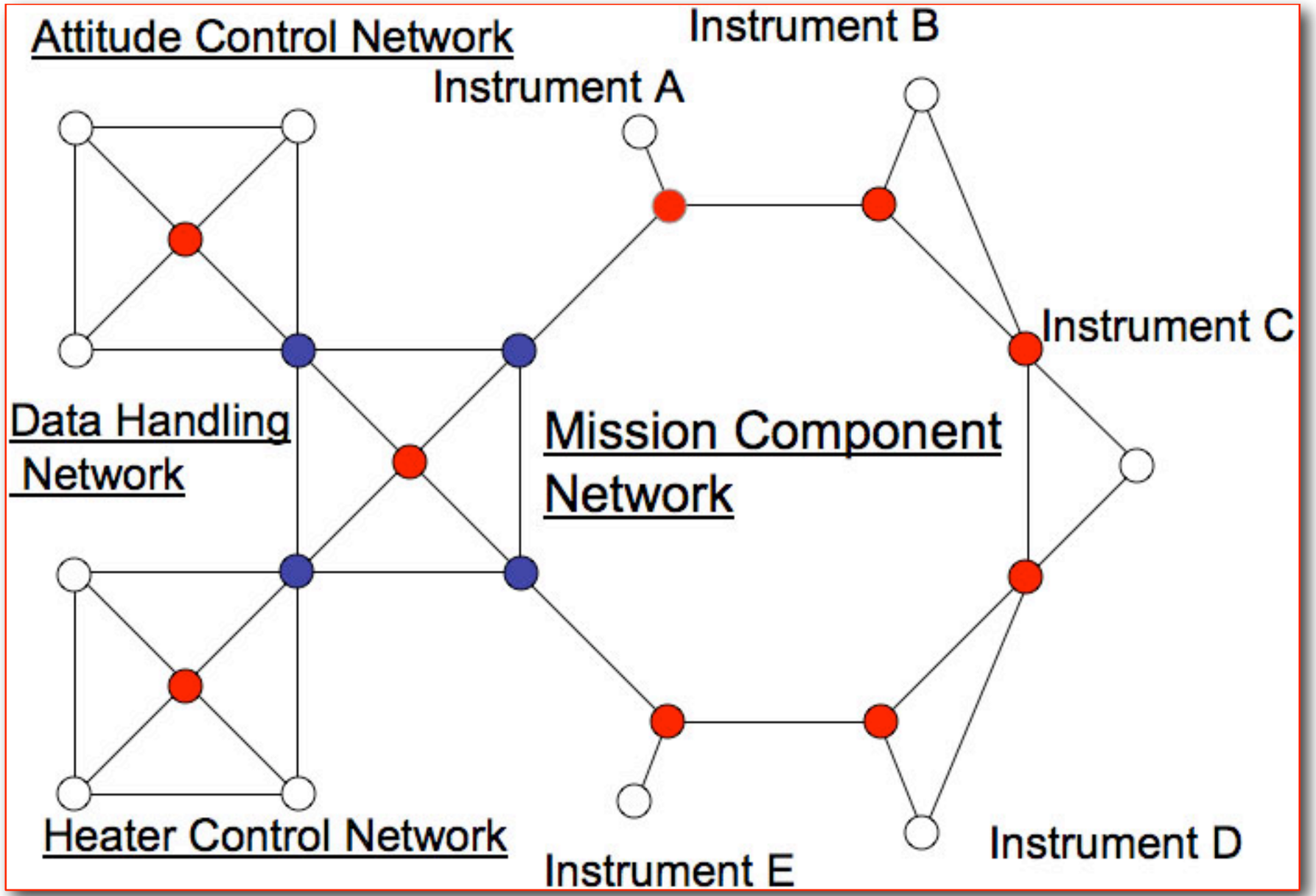
2. Accessibility(RMAP)

3. Re-usability

4. Redundancy

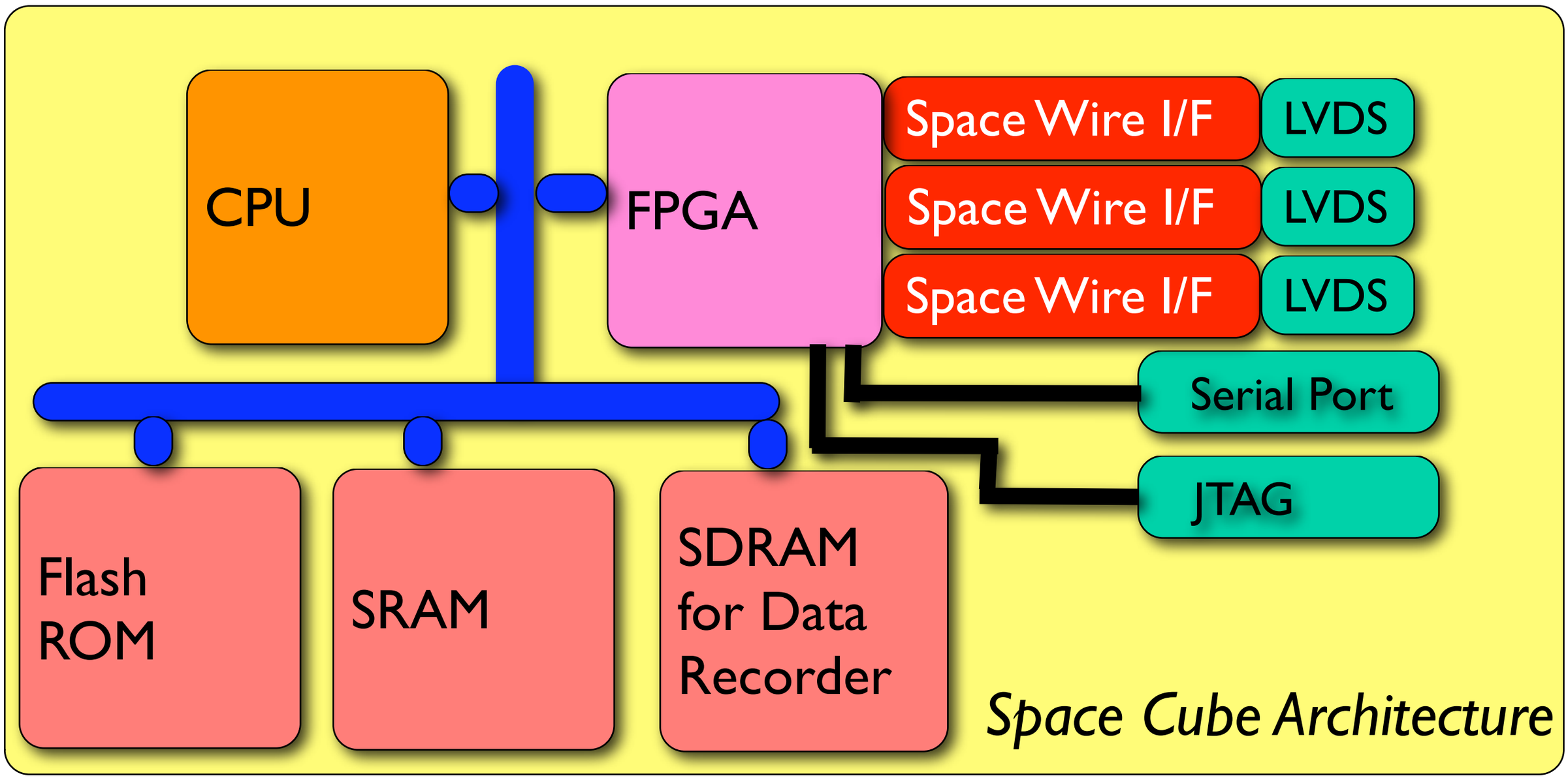
Distributed system

- Intelligent SpW node (Space Cube)
- SpW Router
- non-Intelligent SpW node with SpW I/F chip



Define “Standard Computer” as an intelligent SpW node. → *Space Cube*

= a minimum set of OnBoard Computer

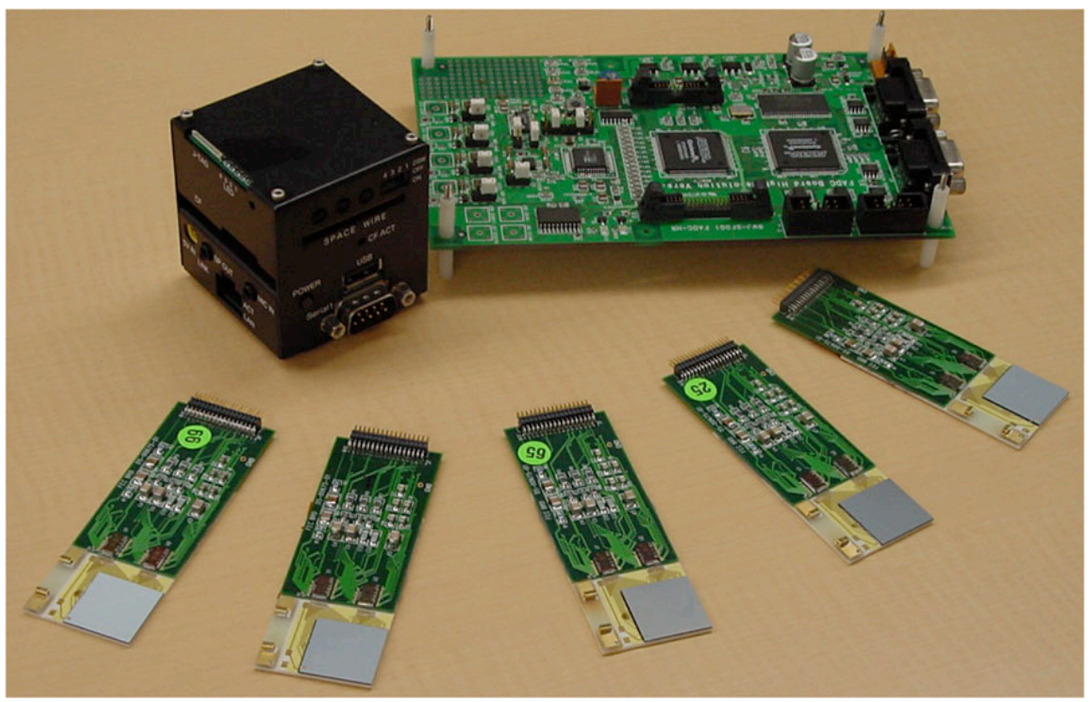


Support Real Time OS, such as TRON/T-Kernel

Space Cube 1

since 2004

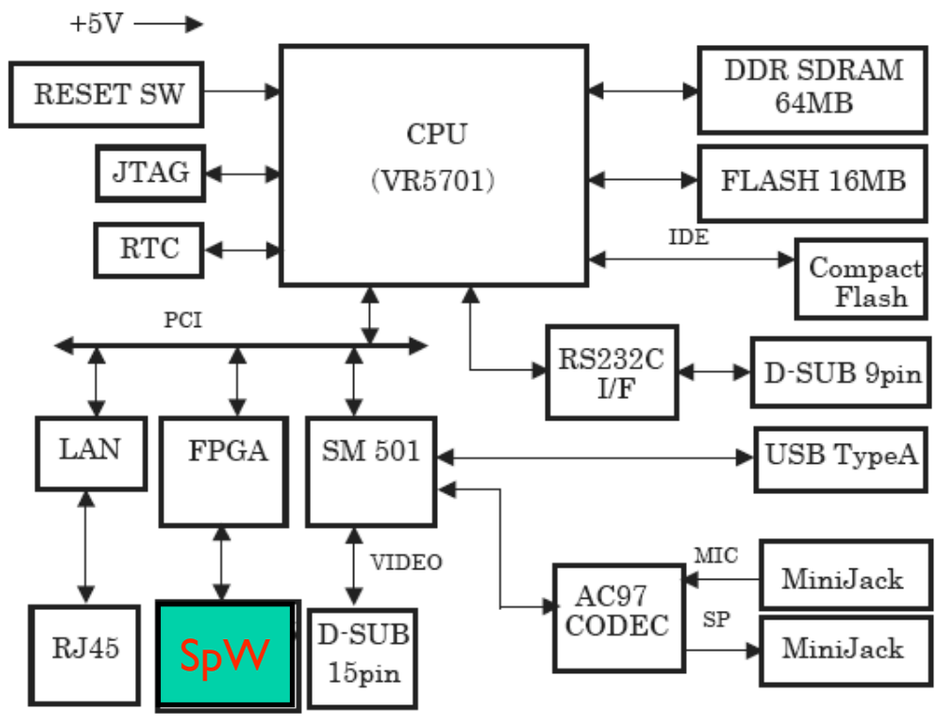
By ISAS/JAXA & Shimafuji.



Compact Space Wire based Computer

Developed to promote SpW based system.
Turns out to be very useful for the demonstration & the education purposes and also "simulating" Space Wire based distributed system.

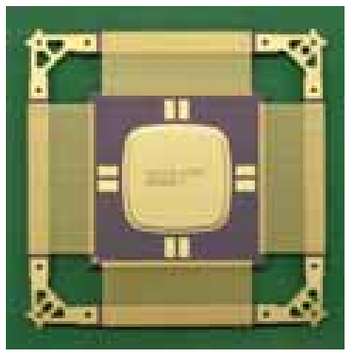
: 3 SpW ports
: Video & USB & Ethernet I/F
: ITRON Real Time OS & Linux
: Set of I/O modules for real applications on ground

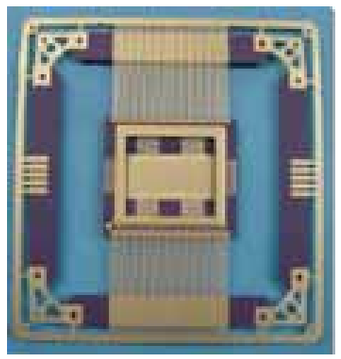


Space Cube 2

Flight Computer for Space (JAXA/NTS)

CPU	**HR5000 (64 bit, 32 MHz Operation)**
Space Wire I/F	**3ch**
System Memory	**2 MB Flash Memory**
	4 MB Burst SRAM
	4 MB Asynchronus SRAM
Data Recorder Memory	**1 GB Asynchronus SDRAM**
	1 GB Flash Memory
Size	**71 (W) x 220.5 (D) x 170.5 (H)**
Weight	**1.9 kg**
Power	**7 W**

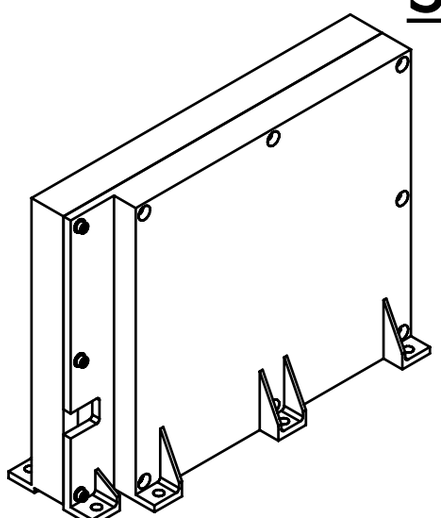


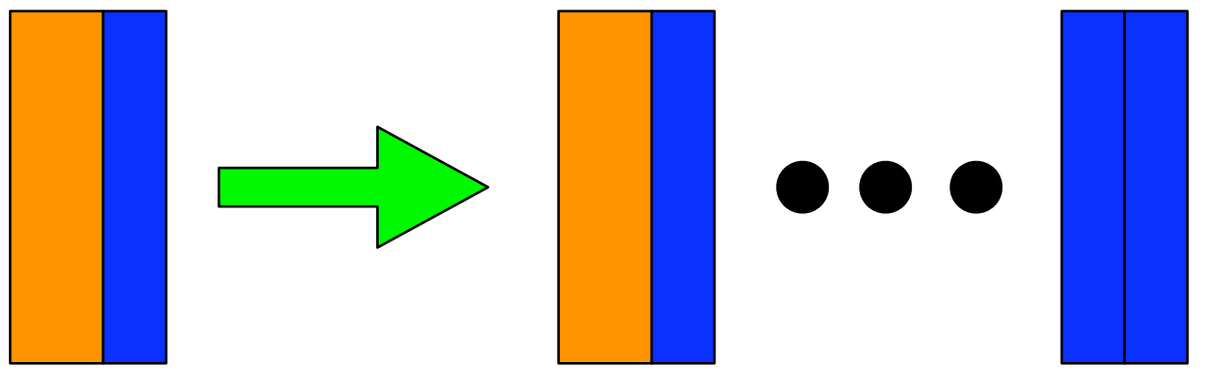


HR5000 micro controller and Bust SRAM

Max 200 MHz

Stack Configuration





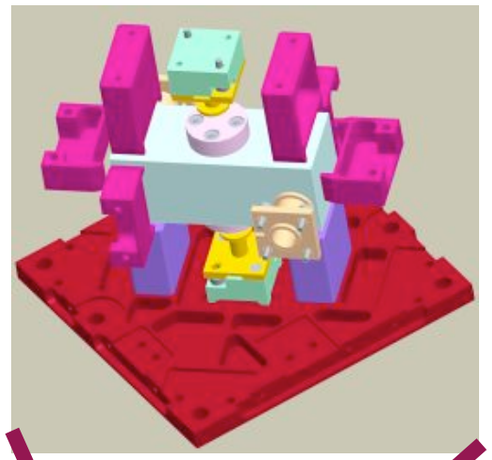
Space Cube 2 on **SDS-1** (JAXA's Engineering Piggyback Satellite) **Launch 2008-Aug**

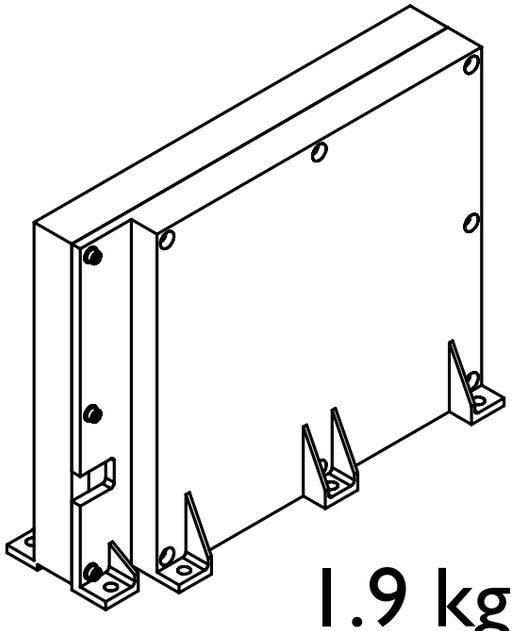
- SDS-1 carries
  SWIM (SpaceWire Interface test Module (JAXA/NTS/MHI)
  SpaceCube 2 and a sub-module for small experiments

100 kg

Small Experiments
(Prototype for future)
Gravitational Wave Exp.
by U.Tokyo Group)

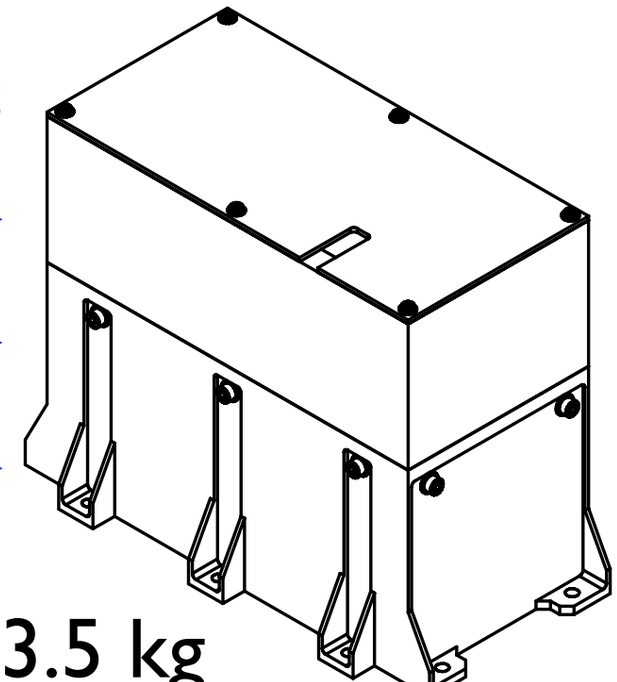
Test Mass



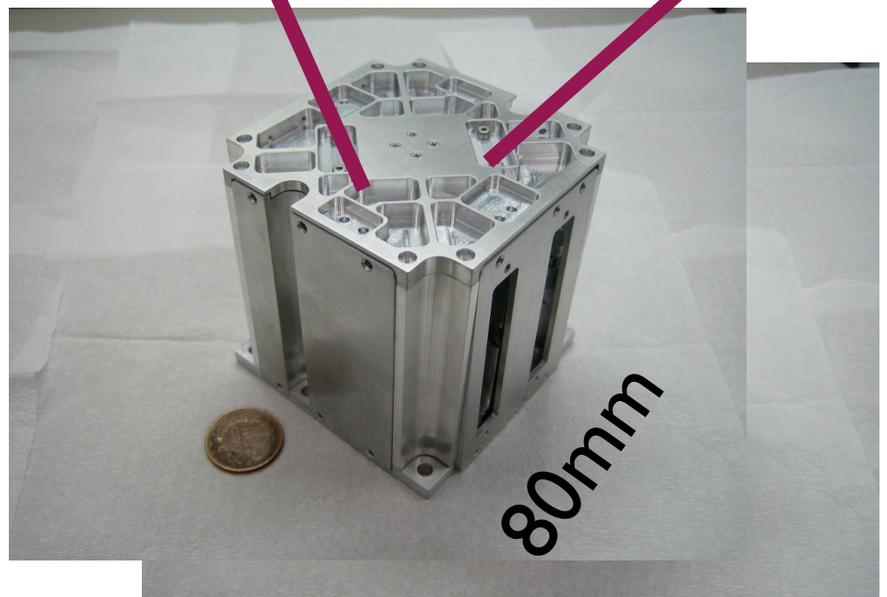


1.9 kg

Space Wires



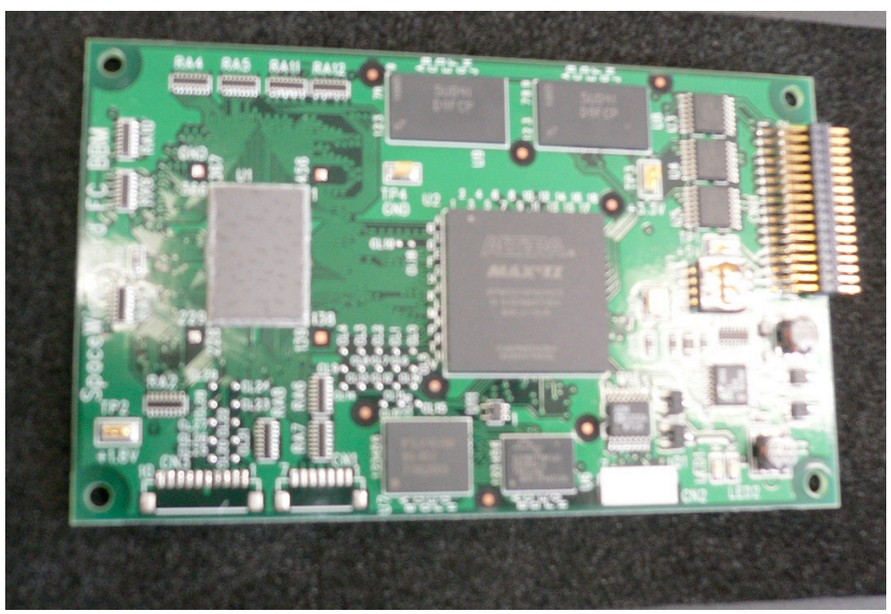
3.5 kg



More for future SpW-based satellites

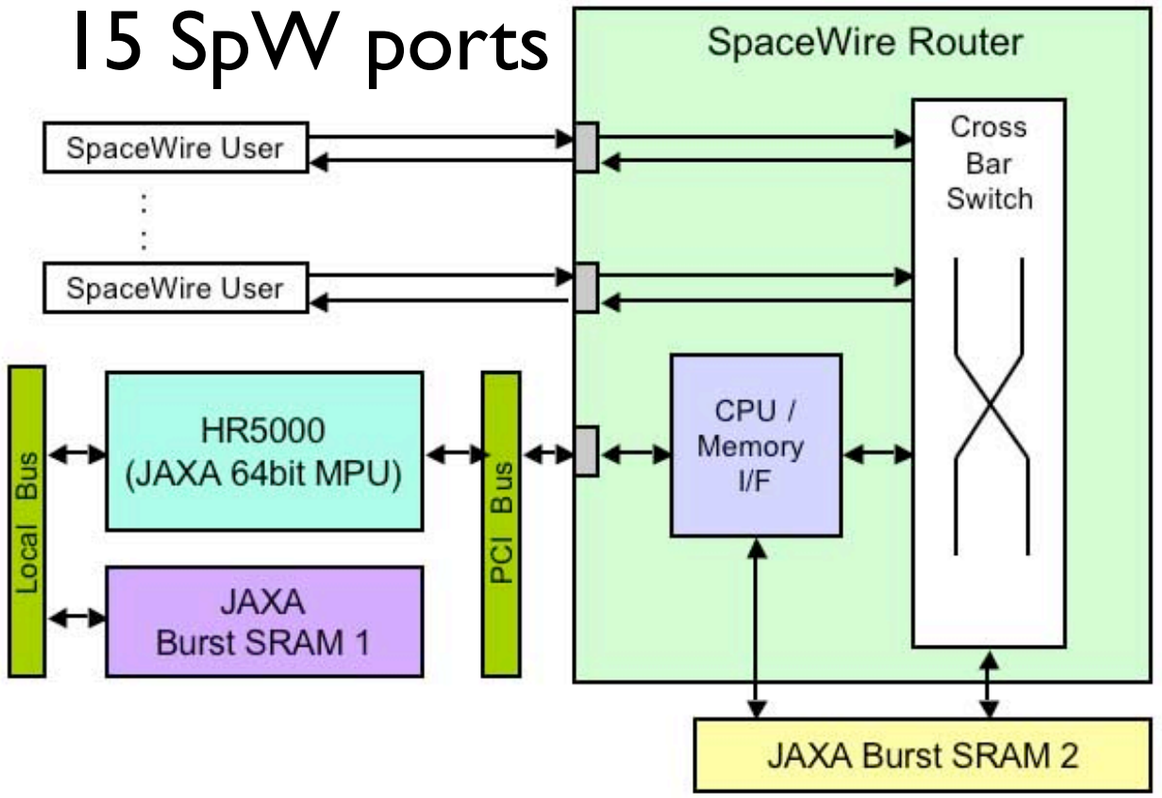
Space Card_MHI

- Based on Space Cube Architecture
- SOI-based New RISC-type 32bit CPU (for Space)
- Very Compact
  (best for small satellites)
- Will be used as computers for mission components in the NeXT (New X-ray Telescope) mission.



MHI&JAXA
(see MHI booth)

Router ASIC
(NEC&JAXA)



SpW I/F ASIC
(NEC&JAXA)

parallel bus + DMA

Summary

- Space Wire standard has been adopted by ISAS for science missions (see also Matsuda et al. this conf.).
- We define Space Cube architecture to clarify minimum specifications as a standard OBC.
- The combination of *Space Cube 1* on the ground and *Space Cube 2* in the space provides us with a user-friendly platform for the development of satellites (see Yuasa et al, Odaka et al.). *Space Cube 2* will be used in a series of small scientific satellites in ISAS and also in mid-scale satellites such as NeXT.
- Further development includes *Space Card*, Router Chip and Space Wire I/F chip.